Introducing 65 nm technology in Microwind3

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This paper describes the improvements related to the CMOS 65 nm technologies and the implementation of this technology in Microwind3. The main novelties related to the 65 nm technology such as enhanced strained silicon, process options and low-K dielectrics are described.

1. Recent trends in CMOS technology

Firstly, we give an overview of the evolution of important parameters such as the integrated circuit (IC) complexity, the gate length, switching delay and supply voltage with a prospective vision down to the 22 nm CMOS technology. The trend of CMOS technology improvement continues to be driven by the need to integrate more functions within a given silicon area. Table 1 gives an overview of the key parameters for technological nodes from 180 nm introduced in 1999, down to 22 nm, which is supposed to be in production around 2011. Demonstration SRAM chips using 45-nm technology have already been made. The goal is to begin manufacturing chips with this technology in late 2007.

Technology node	**180 nm**	**130 nm**	**90 nm**	**65 nm**	**45 nm**	**32 nm**	**22 nm**
First production	1999	2001	2003	2005	2007	2009	2011
Effective gate length	130 nm	70 nm	50 nm	35 nm	25 nm	17 nm	12 nm
Gate material	Poly SiO_2	Poly SiO_2	Poly SiO_2	Poly SiON	Metal High K	Metal High K	Metal High K
Gate atoms	10	8	5	5	5-10	5-10	5-10
Kgates/mm^2	160	240	480	900	1500	2800	4500
Memory point (μ^2)	4.5	2.4	1.3	0.6	0.3	0.15	0.08

Table 1: Technological evolution and forecast up to 2011

The physical gate length is slightly smaller than the technological node, as illustrated in Fig. 1. The gate material has long been polysilicon, with silicon dioxide (SiO_2) as the insulator between the gate and the channel. The atom is a convenient measuring stick for the insulating material transistor beneath the gate. In 90 nm, the gate oxide was consisting of about five atomic layers, equivalent to 1.2 nm in thickness. The thinner the gate oxide, the higher the transistor current and consequently the switching speed. However, thinner gate oxide also means more leakage current. Therefore future technology scaling are expected to be achieved by reducing leakage and improving performance using a number of approaches including the introduction of high-K gate dielectrics with metal gates, or SOI with multi-gate transistor architectures.

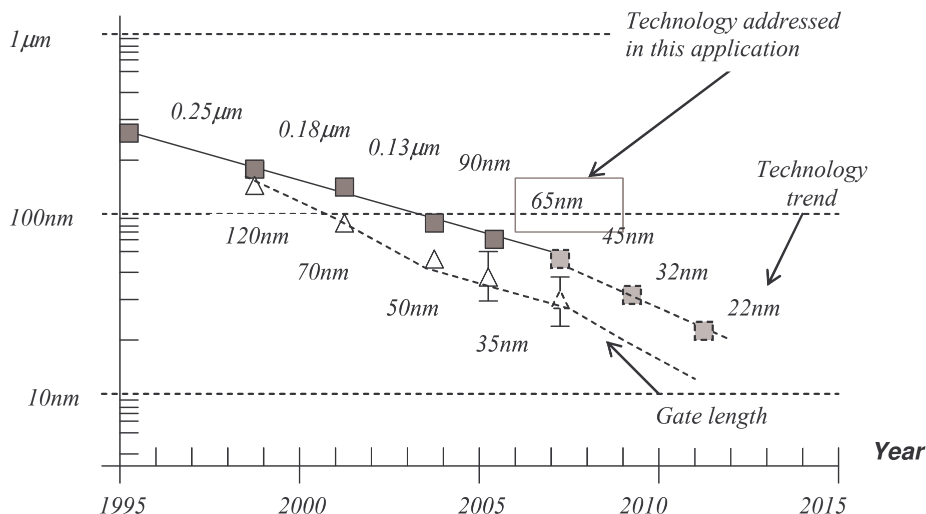


Figure 1: The technology scale down towards nano-scale devices

At each lithography scaling, the linear dimensions are approximately reduced by a factor of 0.7, and the areas are reduced by factor of 2. Smaller cell sizes lead to higher integration density which has risen to nearly 1 million gates per mm^2 in 90 nm technology.

The integrated circuit market has been growing steadily since many years, due to ever-increased demand for electronic devices. The production of integrated circuits for various technologies is illustrated over the years in Fig. 2. It can be seen that a new technology has appeared regularly each two years, with a ramp up close to three years. The production peak is constantly increased, and similar trends should be observed for novel technologies such as 65nm (forecast peak in 2009).

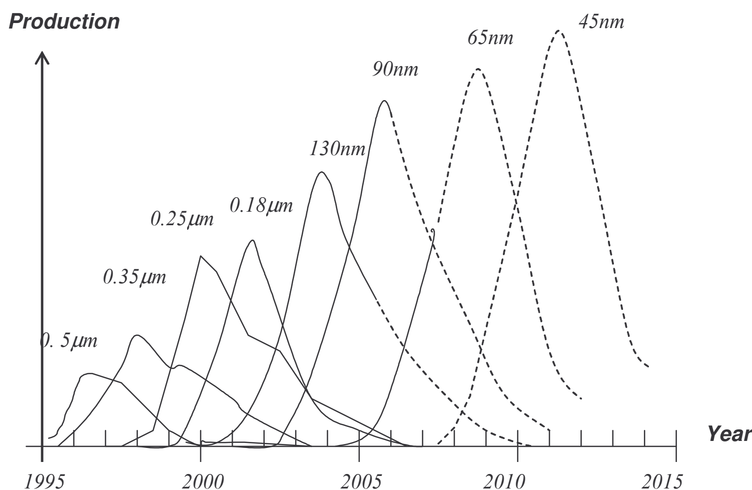


Figure 2: Technology ramping every two years, adapted from [8]

The industrial 90-nm process from Intel was presented by Ghani in a paper in IEDM 2003 [2]. It features the introduction of uniaxial tensile strain in the NMOS transistor channel and uniaxial compressive strain in the PMOS transistor channel resulting in dramatic improvements in channel mobility and consequently drive currents. More information about the implementation of the 90-nm technology may be found in the Microwind application node [10].

2. Introducing the 65 nm technology

Industrial 65-nm processes have been introduced by Toshiba in 2002 [3], Fujitsu [5], NEC [6] and STMicroelectronics [7] in 2003, and by Intel in 2004 [8]. Other companies, such as IBM, TI, Motorola, TSMC, Samsung presented the results of integrated 65nm processes at conferences or features of their 65nm technology in 2003-2004 time frame. With transistor channels ranging from 30 nm to 50 nm in size (30 to 50 billionths of a meter), comparable to the smallest micro-organisms, this technology is truly a nanotechnology. Some of the features of the 65 nm technologies from various providers are given in Table 2.

Feature	**Foundry**				
	Intel	**ST Microelectronics**	**Fujitsu**	**Toshiba**	**NEC**
V_{DD} (V)	1, 1.2	0.9/1.1	1-1.2	0.85	0.9-1.2
Effective gate length (nm)	35	45	30/50	30	43
Oxide thickness (nm)	1.2	1.2	1.1-1.7	1.0	1.1-1.35
# of metal layers	8		12	up to 13	
Interconnect layer permittivity K	2.9		2.25~2.9	2.7	2.5~2.9
Reference	[8]	[7]	[5]	[3]	[6]

Table 2: Features of the 65 nm technology

Compared to 90nm technology, most 65nm technologies offer:

- 1.3 times faster speed
- 0.6 times lower power
- 2 times higher density

65-nm process variants

There may exist several variants of the 65-nm process technology. One corresponds to the highest possible speed, at the price of a very high leakage current. This technology is called “High speed” as it is dedicated to applications for which the highest speed is the primary objective: fast microprocessors, fast DSP, etc. This technology has not been addressed in Microwind’s 65nm rule file.

The second technological option called “General Purpose” (Fig. 3) is targeted to standard products where the speed factor is not critical. The leakage current is one order of magnitude lower than for the high-speed variant, with gate switching decreased by 50%.

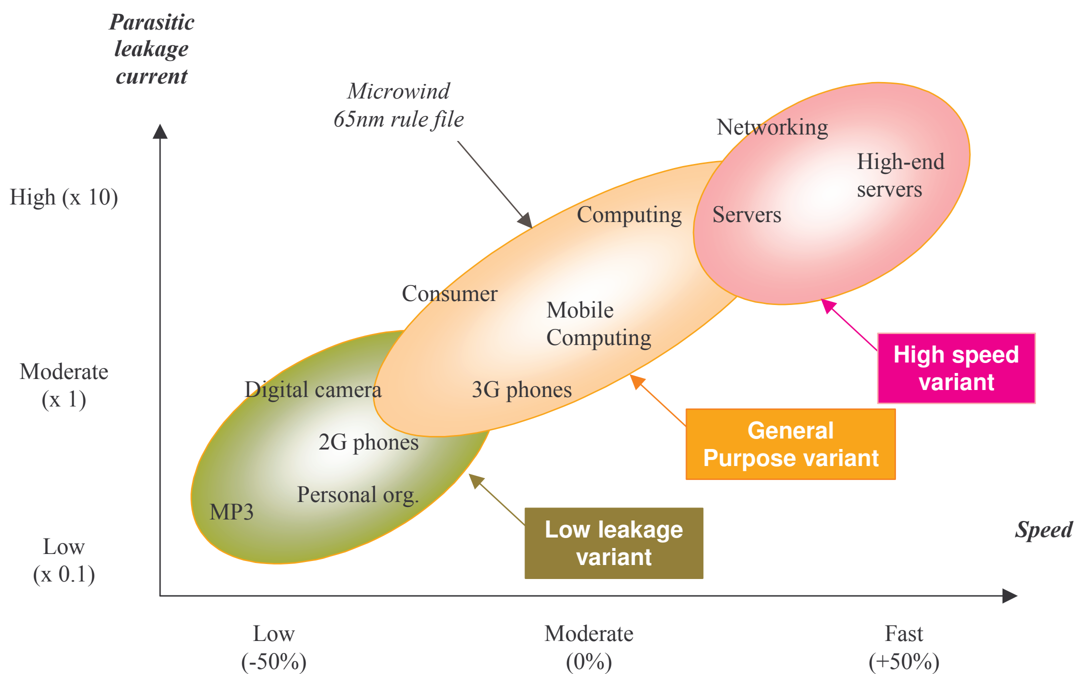


Figure 3: Introducing three variants of the 65nm technology

There may also exist a third variant called low leakage (bottom left of fig. 3). This variant concerns integrated circuits for which the leakage must remain as low as possible, a criterion that ranks first in applications such as embedded devices, mobile phones or personal organizers.
The operational voltage is usually from 0.85V to 1.2V, depending on the technology variant. In Microwind, we decided to fix VDD at 1.0V in the cmos65nm.RUL rule file, which represents a compromise between all possible technology variations available for this 65-nm node.

Gate dielectric

Continued thickness reduction of conventional oxides such as silicon dioxide (SiO_2) results in reliability degradation and unacceptable current leakage. New dielectric materials with high permittivity (High-"K") are needed to replace SiO2, both for the MOS device itself and the embedded capacitors. Silicon oxynitride (SiOxNy) has been proposed in 65nm technologies as an effective replacement to SiO2 as the dielectric material in metal-oxide-semiconductor devices (figure 4). Depending on the Oxygen/Nitrogen ratio, the oxynitride film dielectric permittivity may be adjusted.

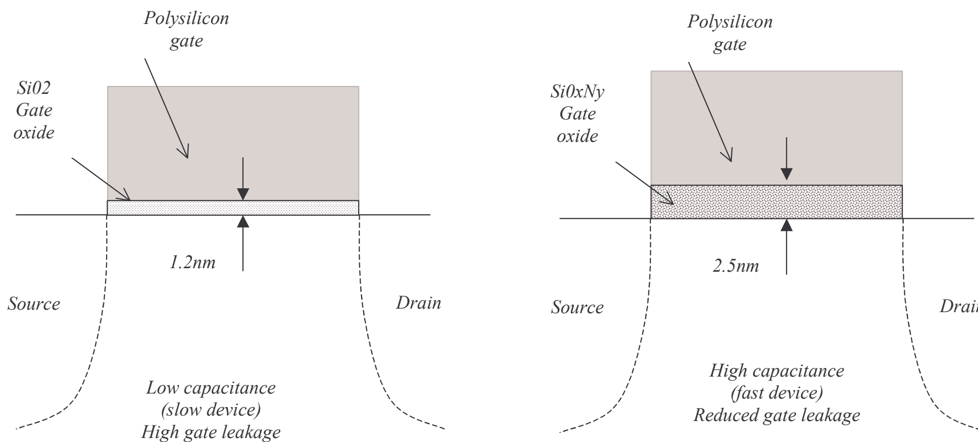


Figure 4: The new gate oxide material enhances the MOS device performances in terms of switching speed and leakage

Strained Silicon

The main novelty related to the 90 and 65 nm technology is the introduction of strained silicon to speed-up the carrier mobility, which boosts both the n-channel and p-channel transistor performances. In Intel's the 65 nm technology [8] the channel strains in both NMOS and PMOS devices have been improved over 90 nm technolgy. PMOS transistor channel strain has been enhanced by increasing the Ge content in the compressive SiGe film. Both transistors employ ultra shallow source-drains to further increase the drive currents.

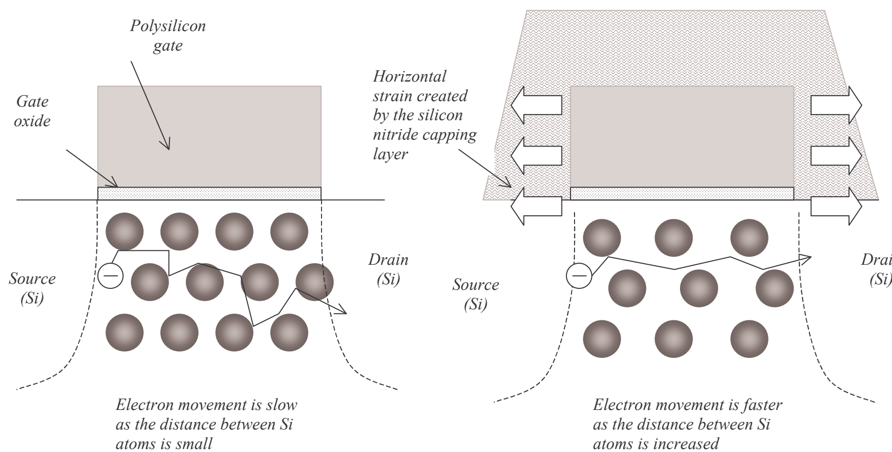


Figure 5: Strain generated by a silicon-nitride capping layer which increases the distance between atoms underneath the gate, which speeds up the electron mobility of n-channel MOS devices

Let us the silicon atoms forming a regular lattice structure, inside which the electrons participating to the device current have to flow. In the case of electron carriers, stretching the lattice allows the charges to flow faster from the drain to the source, as depicted in Fig. 5.

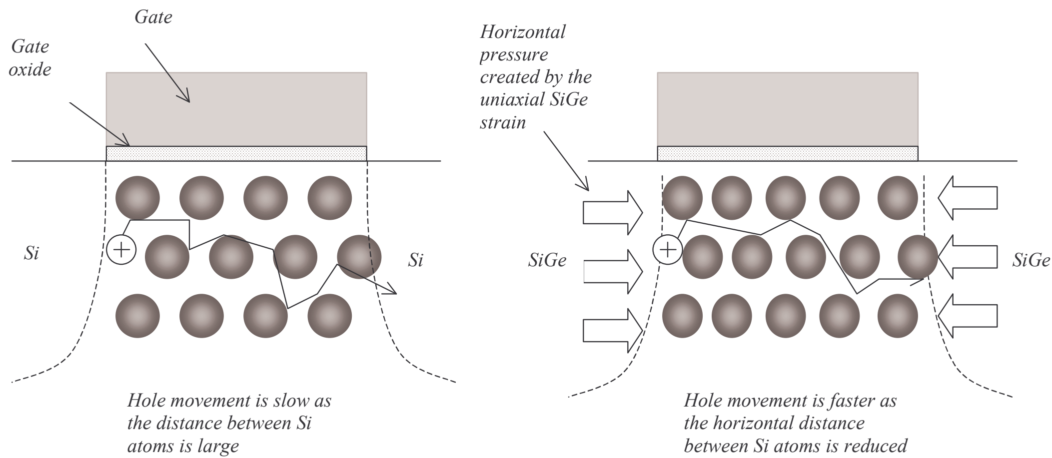


Figure 6: Compressive stain to reduce the distance between atoms underneath the gate, which speeds up the hole mobility of p-channel MOS devices

The mobility improvement exhibits a linear dependence with the tensile film thickness. A 80 nm film has resulted in a 10% saturation current improvement in Intel's 90nm technology [2]. The strain may also be applied from the bottom with a uniform layer of an alloy of silicon and germanium (SiGe).
In a similar way, compressing the lattice slightly speeds up the p-type transistor, for which current carriers consist of holes (Fig. 6). The combination of reduced channel length, decreased oxide thickness and strained silicon achieves a substantial gain in drive current for both nMOS and pMOS devices.

N-channel MOS device characteristics

The tool Microwind in its version 3.1 is configured by default in 65 nm technology. A cross-section of the n-channel MOS devices is given in Fig. 7. The nMOS gate is capped with a specific silicon nitride layer that induces lateral tensile channel strain for improved electron mobility.

Parameter	**NMOS Low leakage**	**NMOS High speed**
Drawn length (m)	70 nm	70 nm
Effective length (m)	50 nm	35 nm
Threshold voltage (V)	0.35	0.25
Ion (A/m)	0.8 mA/µm at VDD=1.0V	1.2 mA/µm at VDD=1.0V
Ioff (A/m)	1 nA	100 nA

Table 3: nMOS parameters featured in the CMOS 65 nm technology provided in Microwind

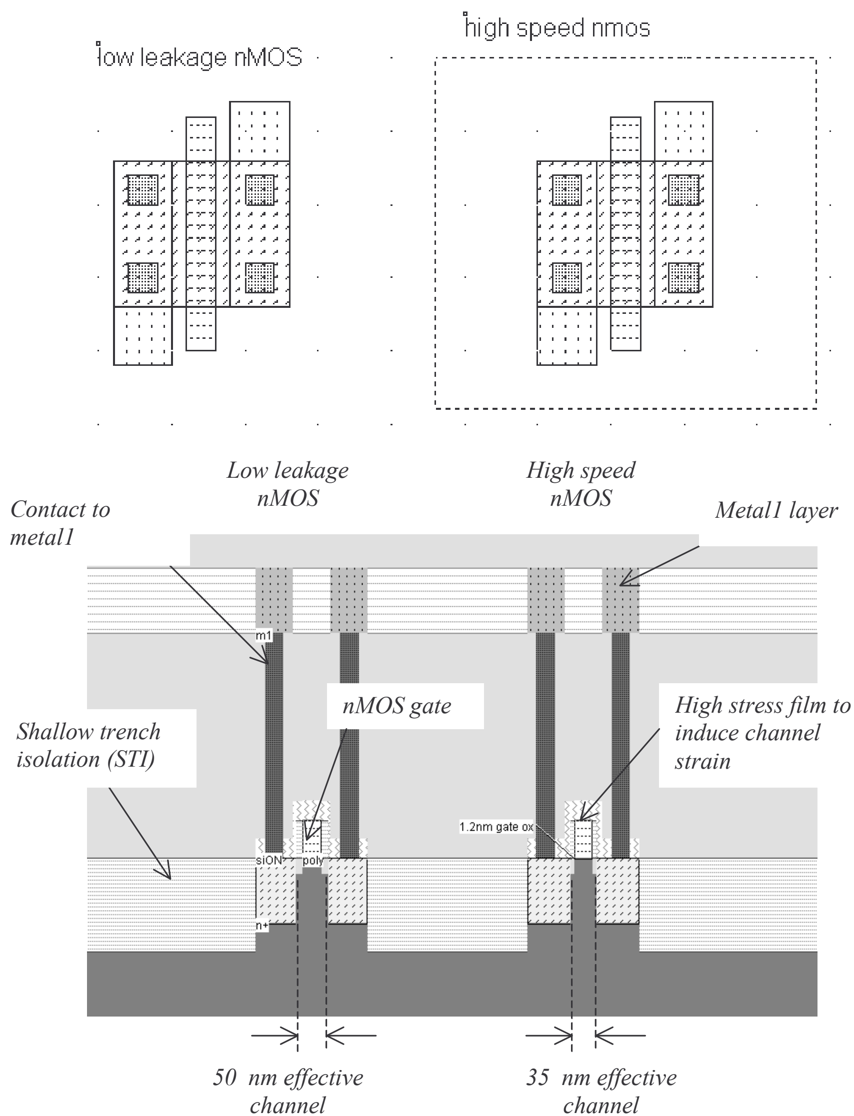
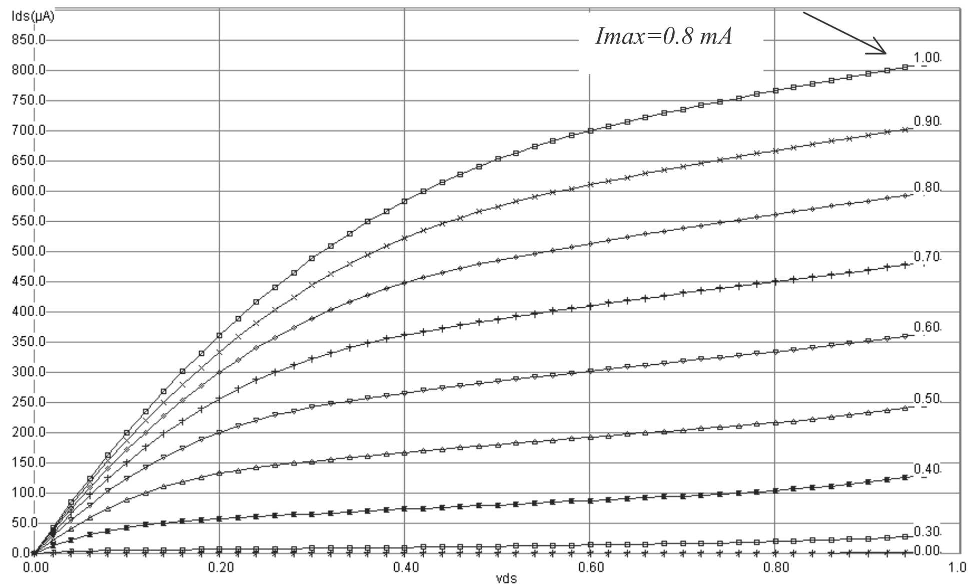
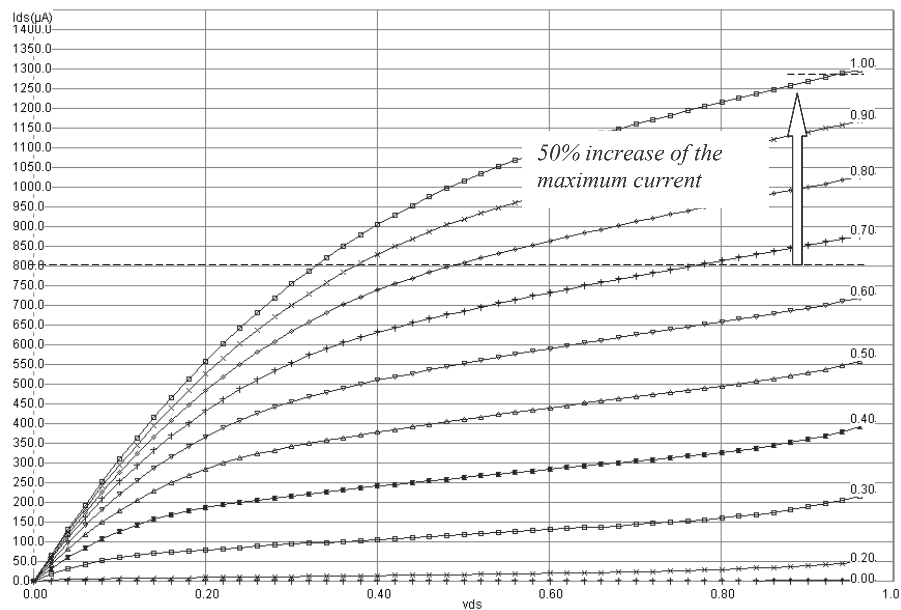


Figure 7: Cross-section of the nMOS devices (allMosDevices.MSK)

The device I/V characteristics of the low-leakage and high-speed MOS devices listed in Table 3 are obtained using the MOS model BSIM4 (See Sicard's book [1] for more information about this model). The cross-section of the low-leakage and high-speed MOS devices do not reveal any major difference (Fig. 7), except a reduction of the effective channel length. Concerning the low-leakage MOS, the I/V characteristics reported in Fig. 8 demonstrate a drive current capability around 0.8 mA for W=1.0µm at a voltage supply of 1.0 V. For the high speed MOS, the effective channel length is slightly reduced as well as the threshold voltage, to achieve an impressive drive current around 1.2 mA/µm.

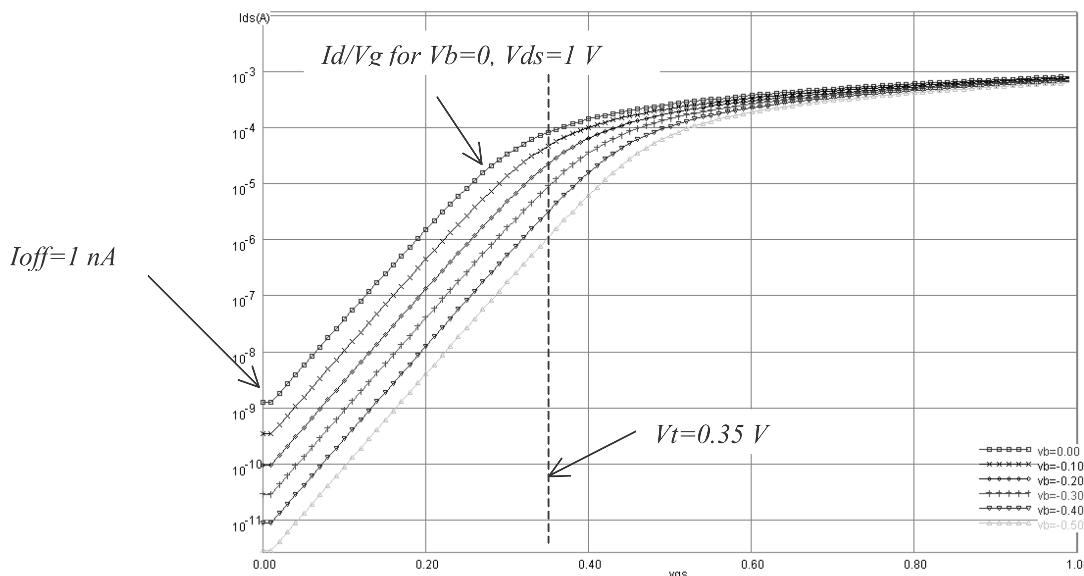


Low leakage W=1µm, Leff= 50nm

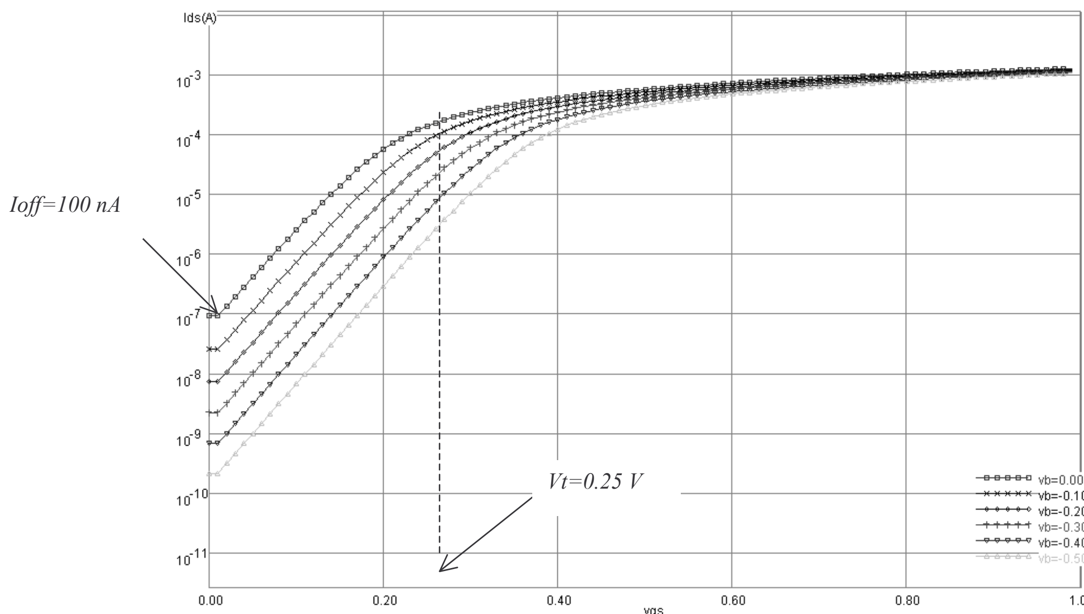


(b) High speed W=1µm, Leff= 35nm

Figure 8: Id/Vd characteristics of the Low leakage and high speed nMOS devices



(a) Id/Vg characteristics for low leakage MOS (W=1 µm, Leff=50 nm)



(b) Id/Vg characteristics for high speed MOS (W=1 µm, Leff=35 nm)

Figure 9: Id/Vg characteristics (log scale) of the Low leakage and high-speed nMOS devices

The drawback of the astounding high-speed MOS current drive is the leakage current which rises from 1 nA/µm (Low leakage) to 100 nA/µm (High speed), as seen in the Id/Vg curve at the X axis location corresponding to Vg= 0 V (Fig. 9). Notice that the threshold voltage Vt is significantly higher for the low leakage MOS than for the high speed MOS.

P-channel MOS device characteristics

The PMOS drive current in this 65 nm technology is around 450 µA/µm for the low-leakage MOS and up to 700 µA/µm for the high-speed MOS. These values (See Table 4) are not particularly high, as the target applications for this technology is low-power, in contrast to Intel's 65-nm technology targeted to high-speed digital circuits such as microprocessors (see fig. 3 for an illustration of 65-nm technology variants). The leakage current is remarkably low, around 1 nA/µm for the low-leakage MOS and near 100 nA/µm for the high-speed device. The cross-section of the pMOS device reveals an SiGe material that induces compressive strain to obtain maxiumum current capabilities near 0.7 mA/µm (Fig. 10).

Parameter	**pMOS Low leakage**	**pMOS High speed**
Drawn length	70 nm	70 nm
Effective length	50 nm	35 nm
Threshold Voltage (V)	0.35 V	0.25 V
Ion (A/m)	0.45 mA/µm	0.7 mA/µm
Ioff (A/m)	1 nA/µm	100 nA/µm

Table 4: pMOS parameters featured by the 65 nm CMOS technology provided in Microwind

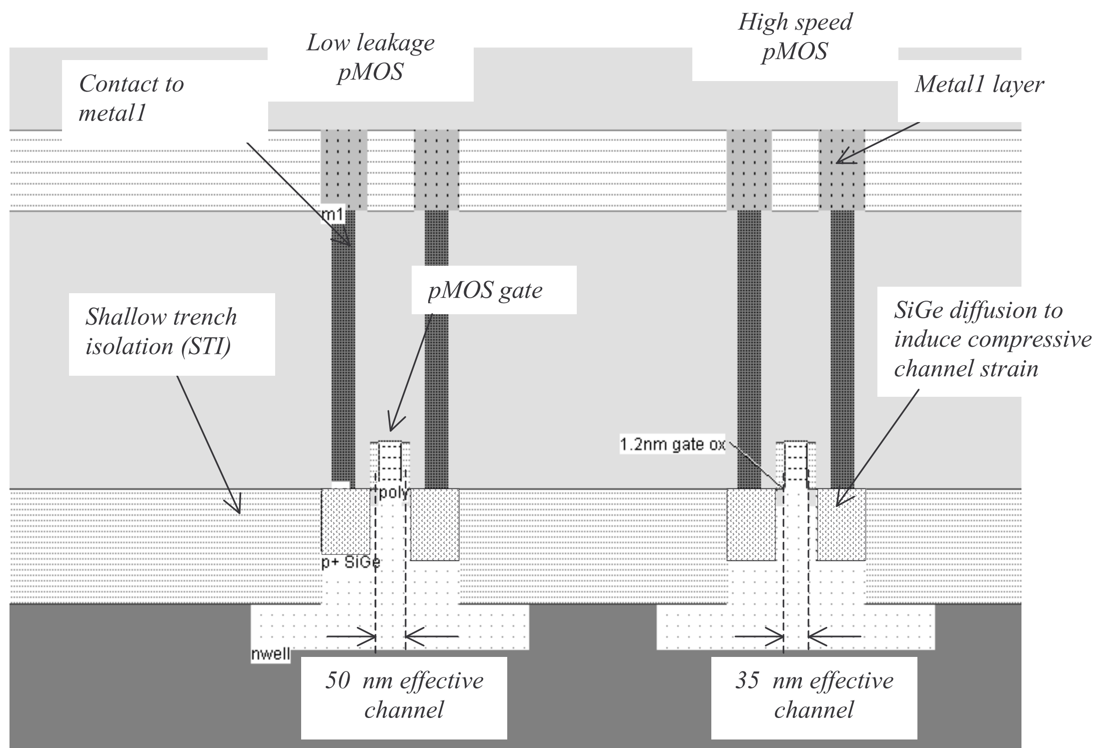


Figure 10: Cross-section of the pMOS devices

Metal Layers

As seen in the palette (fig. 11), the available metal layers in 65nm technology range from *metal1* to *metal8*. The layer *metal1* is situated at the lowest altitude, close to the active device, while *metal8* is nearly 10µm above the silicon surface. Metal layers are labeled according to the order in which they are fabricated, from the lower level (*metal1*) to the upper level (*metal8*).

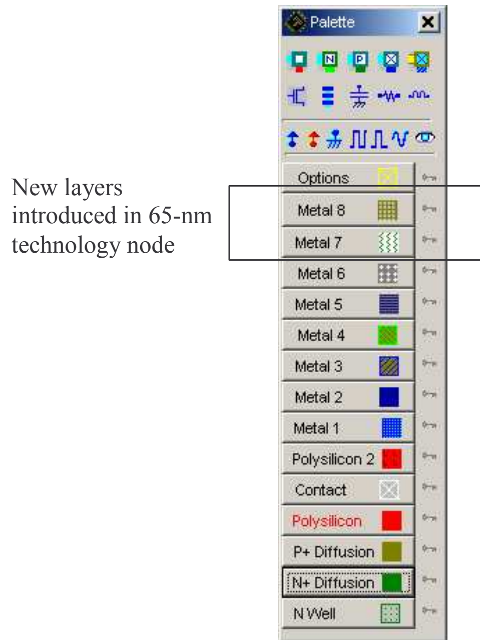


Figure 11: Microwind window with the palette of layers including 8 levels of metallization

In Microwind, specific macros are accessible to ease the addition of contacts in the layout. These macros may be found in the palette. As an example, you may instantiate a design-error free *metal7/metal8* contact by selecting *metal8*, followed by a click on the upper left corner icon in the palette. Additionally, an access to complex stacked contacts is proposed thanks to the icon "complex contacts" situated in the palette, second row, second column. The screen reported in figure 13 appears. By default you create a contact from poly to *metal1*, and from *metal1* to *metal2*. Change the tick to build more complex stacked contacts.

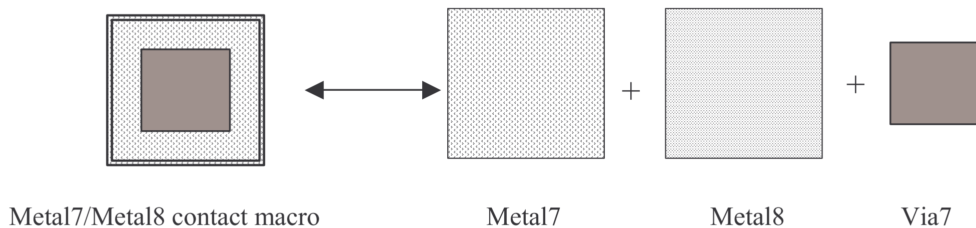


Figure 12: Access to contact macros between metal layers

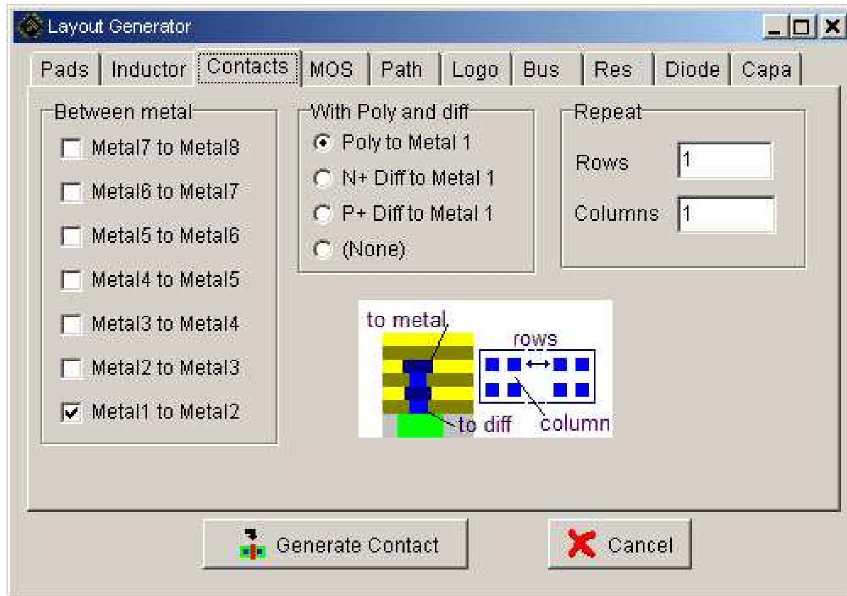


Figure 13: Access to complex contact generator

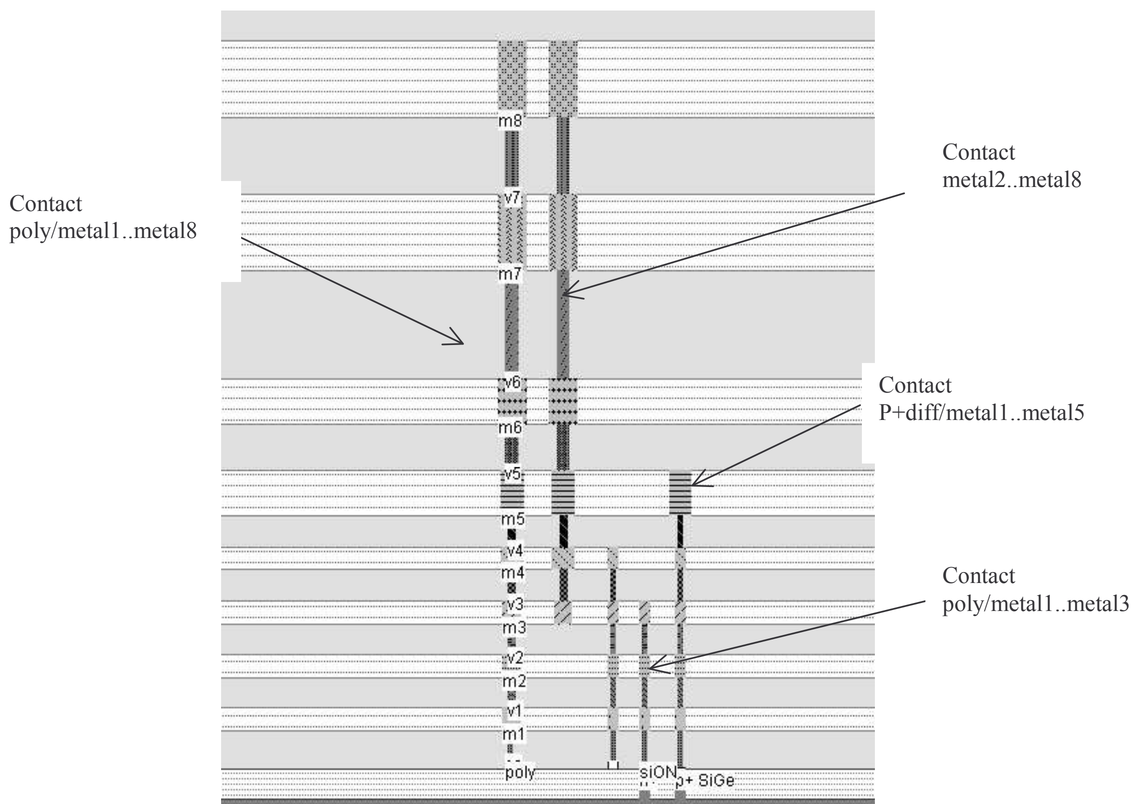


Figure 14: Examples of layer connection using the complex contact command from Microwind (Contacts.MSK)

Each layer is embedded into a low dielectric oxide (referred as interconnect layer permittivity K in table 2) which isolates layers from each other. A cross-section of a 65nm CMOS technology is shown in figure 14. In 65nm technology, the layers *metal1..metal4* have almost identical characteristics. Concerning the design rules, the minimum size *w* of the interconnect is 3 λ. The minimum spacing is 4 λ. Layers *metal5* and *metal6* are a little larger, while layers *metal7* and *metal8* are significantly thicker and larger, to drive high currents for supplies.

Ring Inverter Simulation

The ring oscillator made from 5 inverters has the property of oscillating naturally. We observe in the circuit of figure 15 the oscillating outputs and measure their corresponding frequency.

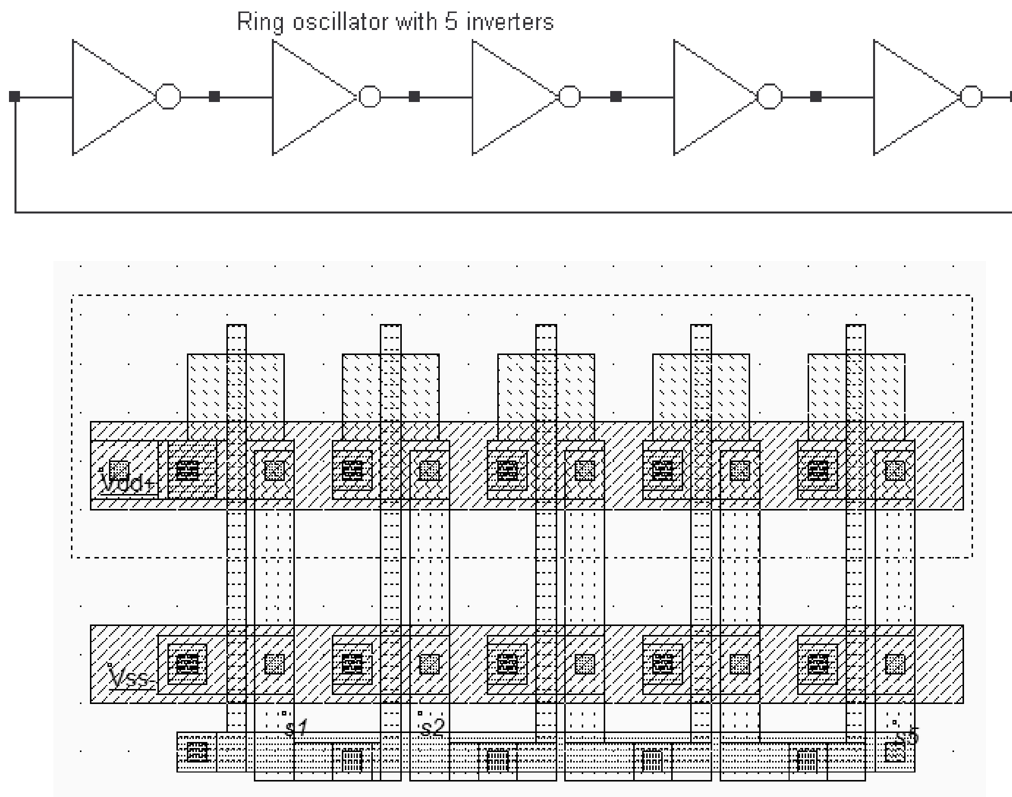
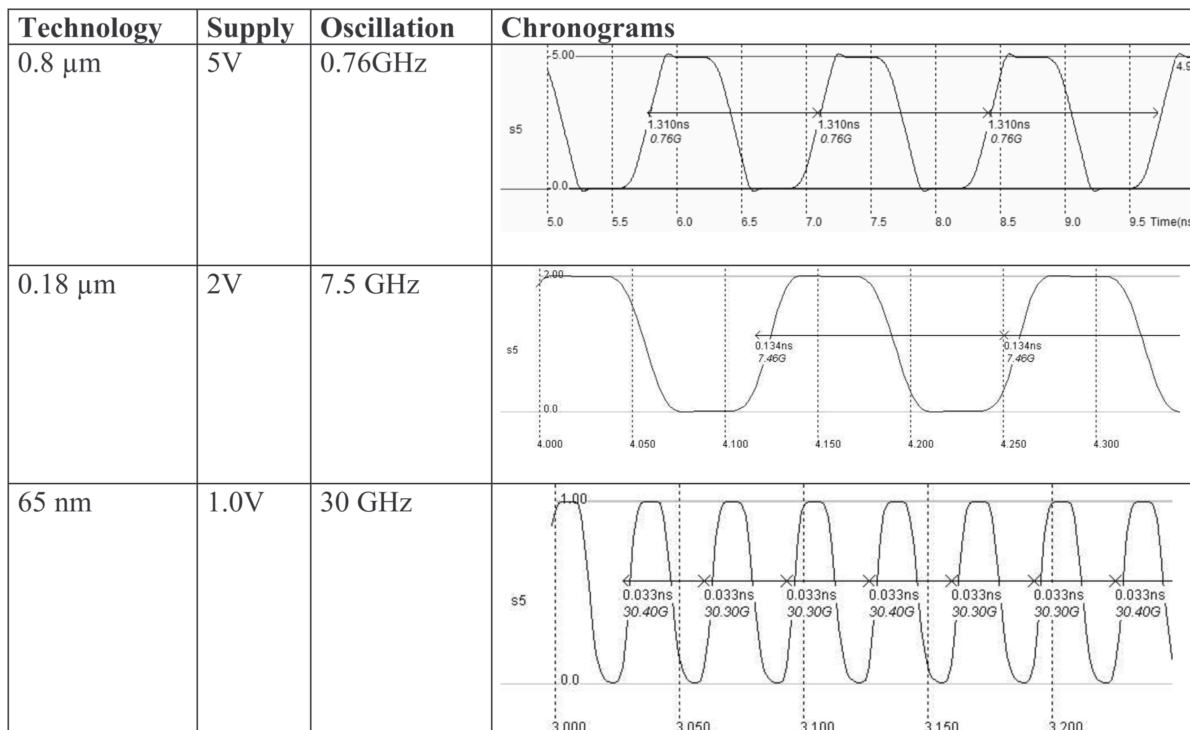


Figure 15: Schematic diagram and layout of the ring oscillator used for simulation (INV5.MSK)

The ring oscillator circuit can be simulated easily at layout level with Microwind using various technologies. The time-domain waveform of the output is reported in figure 16 for 0.8, 0.12µm and 65nm technologies. Although the supply voltage (VDD) has been reduced (VDD is 5V in 0.8µm, 1.2V in 0.12µm, and 1.0 V in 65nm), the gain in frequency improvement is significant.



Technology	Supply	Oscillation	Chronograms
0.8 µm	5V	0.76GHz	
0.18 µm	2V	7.5 GHz	
65 nm	1.0V	30 GHz	

Figure 16: Oscillation frequency improvement with the technology scale down (Inv5.MSK)

Use the command **File → Select Foundry** to change the configuring technology. Select sequentially the **cmos08.RUL** rule file which corresponds to the CMOS 0.8-µm technology, the **cmos018.RUL** rule file (0.18µm technology), and eventually **cmos65nm.RUL** which configures Microwind to the CMOS 65-nm technology. When you run the simulation, observe the change of VDD and the significant change in oscillating frequency.

High Speed vs. Low leakage

Let us consider the ring oscillator with an enable circuit, where one inverter has been replaced by a NAND gate to enable or disable oscillation (Inv5Enable.MSK). The schematic diagram is shown in figure 17, as well as its layout implementation. We analyze the switching performances in high speed and low leakage mode.

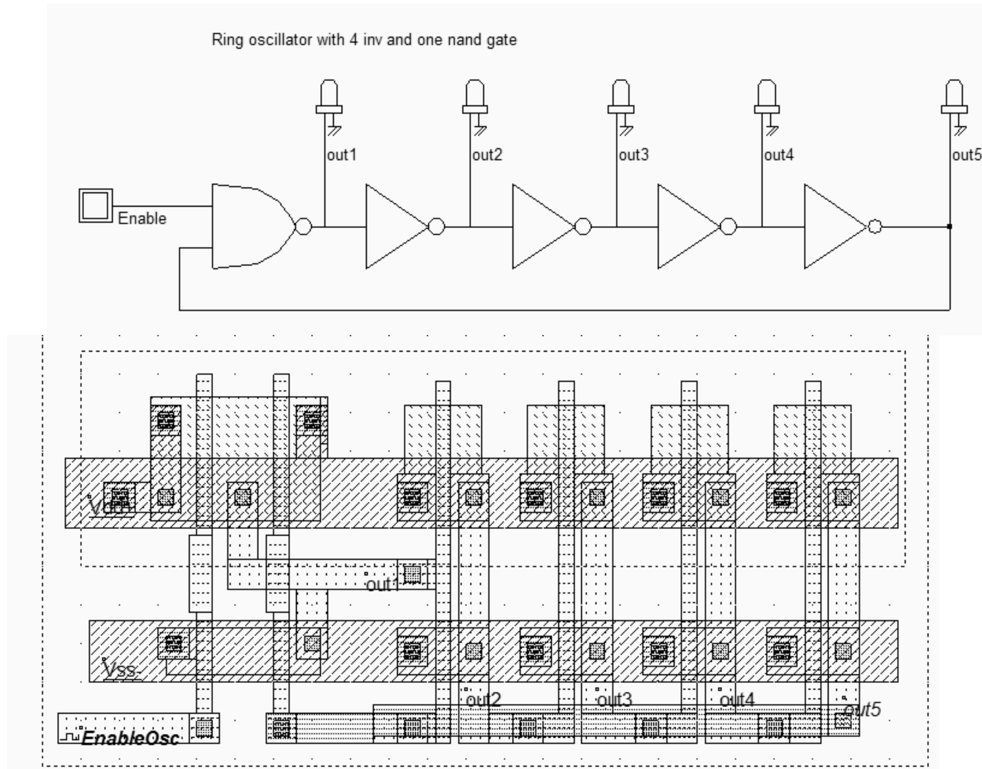


Figure 17 : The schematic diagram and layout of the ring oscillator used to compare the analog performances in high speed and low leakage mode (INV5Enable.MSK)

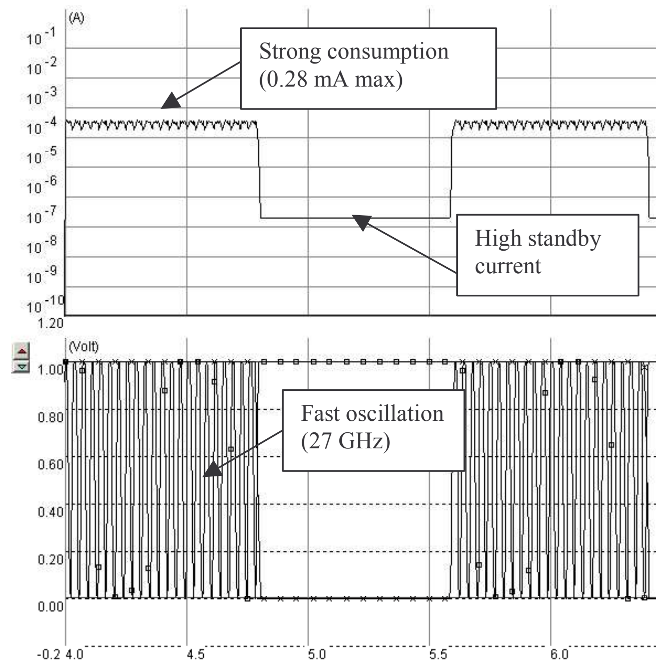


Figure 18: Simulation of the ring oscillator in high speed mode. The oscillating frequency is fast but the standby current is high (Inv5Enable.MSK)

The option layer which surrounds all the oscillator devices is set to high speed mode first by a double click inside that box, and by selecting “high speed” (Fig. 19). The analog performances of both options are summarized in table 5. In high speed mode, the circuit works fast (27 GHz) but consumes a lot of power (0.28 mA) when on, and a significant standby current when off (more than 100 nA), as shown in the simulation of the voltage and current given figure 17. Notice the tick in front of "Scale I in log" to display the current in logarithmic scale.
After changing the properties of the option layer to “low leakage” as shown in Fig. 19, the simulation is performed again. In contrast to “high speed”, the low leakage mode features slower oscillation (16 GHz in figure 20, that is approximately a 40 % speed reduction), with 40 % less current when ON, and nearly two decade less standby current when off (3 nA). In summary, low leakage MOS devices should be used as default devices whenever possible. High speed MOS should be used only when switching speed is critical.

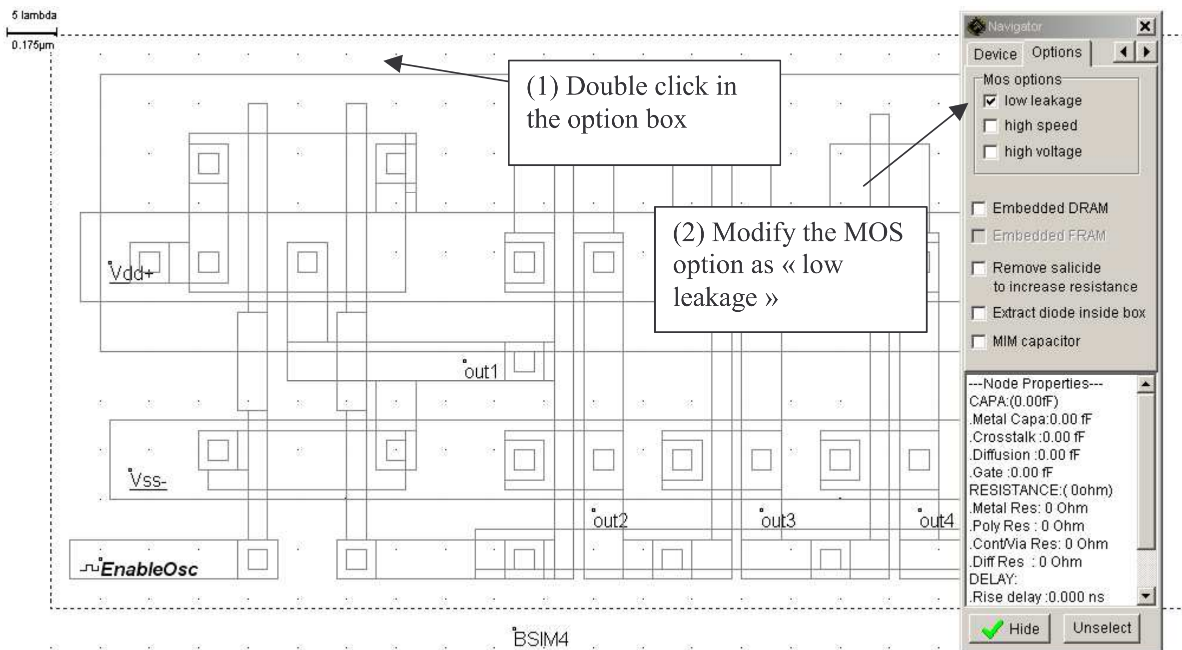


Figure 19: Changing the MOS option into low leakage mode

Figure 20: *Simulation of the ring oscillator in low leakage mode. The oscillating frequency is slower but the standby current is very low (Inv5Enable.MSK)*

Parameter	High Speed mode	Low leakage mode
Maximum current	0.28 mA	0.17 mA
Leakage current	>100 nA	<3 nA
Oscillating frequency	27 GHz	16 GHz

Table 5 : Comparative performances of the ring oscillator (Inv5Enable.MSK)

Conclusion

This application note has illustrated the trends in CMOS technology and introduced the 65 nm technology generation, based on technology information available from integrate circuit manufacturers. A set of specific topics has been addressed, including the new gate dielectric material SiON and the technique called strained silicon for enhanced mobility, the 8-metal interconnect back-end process and the 65-nm process variants. N-channel and P-channel MOS device characteristics have been presented, as well as a comparative study of a ring inverter oscillation for various technologies. Finally, high speed performances have been compared to low leakage, with the impact on speed and leakage current.
Future work will concern the 45nm and 32nm technology nodes, under preparation for an industrial production in 2008.

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