Introducing 90 nm technology in Microwind3

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This paper describes the improvements related to the CMOS 90 nm technologies and the implementation of this technology in Microwind. The main novelties related to the 90 nm technology such as strained silicon, process options and low-K dielectrics are described.

1. Recent trends in CMOS technology

Firstly, we give an overview of the evolution of important parameters such as the integrated circuit (IC) complexity, the gate length, switching delay and supply voltage with a prospective vision down to the 22 nm CMOS technology. The trend of CMOS technology improvement continues to be driven by the need to integrated more functions in a given silicon area. Table 1 gives an overview of key parameters for technological nodes from 180 nm introduced in 1999, downto 22 nm, which is supposed to be in production around 2011.

Technology node	**180 nm**	**130 nm**	**90 nm**	**65 nm**	**45 nm**	**32 nm**	**22 nm**
First production	1999	2001	2003	2005	2007	2009	2011
Gate length	130 nm	70 nm	50 nm	35 nm	25 nm	17 nm	12 nm
Gate material	Poly SiO_2	Poly SiO_2	Poly SiO_2	Poly SiON	Metal High K	Metal High K	Metal High K
Gate atoms	10	8	5	5	5-10	5-10	5-10
Kgates/mm^2	100	200	350	500	900	1500	?
Memory point (μ^2)	4.5	2.4	1.3	0.6	0.3	0.15	0.08

Table 1: Technological evolution and forecast up to 2011

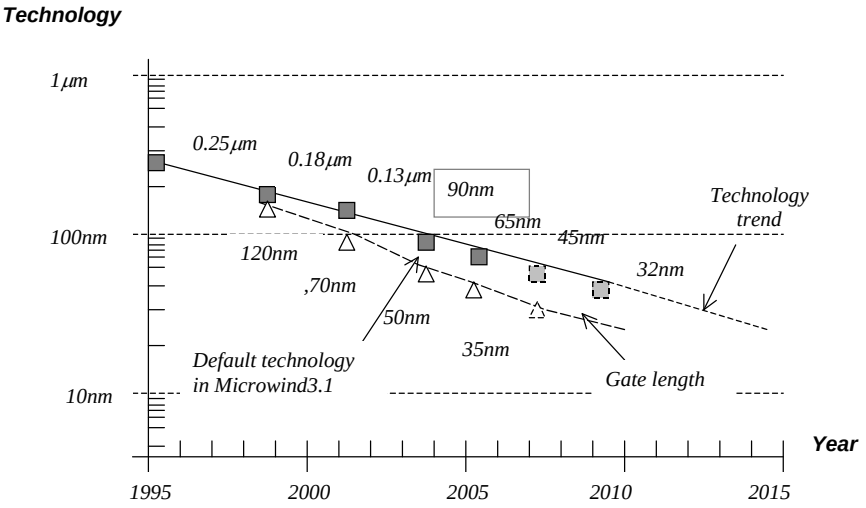


Figure 1: the technology scale down towards nano-scale devices

The physical gate length is slightly smaller than the technological node, as illustrated in Fig. 1. The gate material has long been polysilicon, with silicon dioxide (SiO_2) as the insulator between the gate and the channel. The atom is a convenient measuring stick for the insulating material transistor beneath the gate. In 90 nm, the gate oxide was consisting of about five atomic layers, equivalent to 1.2 nm in thickness. The thinner the gate oxide, the higher the transistor current and consequently the switching speed.

At each lithography scaling, the linear dimensions are approximately reduced by a factor of 0.7, and the areas are reduced by factor of 2. Smaller cell sizes lead to higher integration density which has risen to nearly 1 million gate per mm^2 in 90 nm technology.

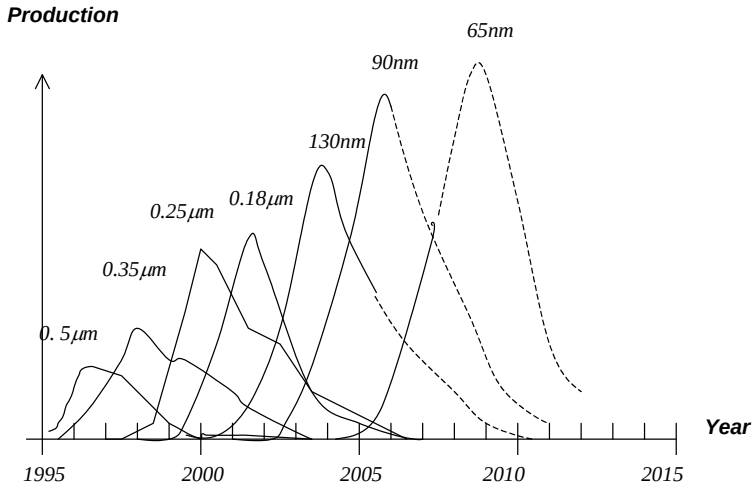


Figure 2: Technology ramping every two years (Adapted from [Ghani])

The integrated circuit market has been growing steadily since many years, due to ever-increased demand for electronic devices. The production of integrated circuits for various technologies is illustrated over the years in Fig. 2. It can be seen that a new technology has appeared regularly each two years, with a ramp up close to three years. The production peak is constantly increased, and similar trends should be observed for novel technologies such as 65nm (forecast peak in 2009).

2. Introducing the 90 nm technology

A complete industrial 90-nm process has first been introduced by Intel in 2003 [Ghani]. With transistor channels around 50 nm in size (50 billionths of a meter), comparable to the smallest micro-organisms, this technology is truly a nanotechnology.

Strained Silicon

The main novelty related to the 90 nm technology is the introduction of strained silicon to speed-up the carrier mobility, which boosts both the n-channel and p-channel transistor performances. It has been known for decades that stretching the silicon lattice improves the carrier mobility, and consequently the device current.

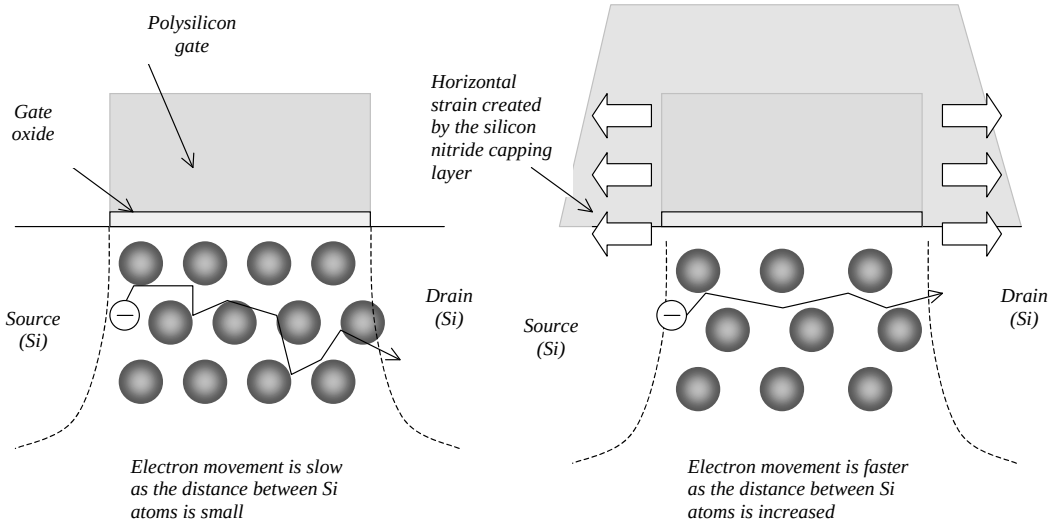


Figure 3: Strain generated by a silicon-nitride capping layer which increases the distance between atoms underneath the gate, which speeds up the electron mobility of n-channel MOS devices

Let us the silicon atoms forming a regular lattice structure, inside which the electrons participating to the device current have to flow. In the case of electron carriers, stretching the lattice allows the charges to flow faster from the drain to the source, as depicted in Fig. 3. The mobility improvement exhibits a linear dependence with the tensile film thickness. A 80 nm film has resulted in a 10% saturation current improvement in Intel's 90nm technology [Ghani]. The strain may also be applied from the bottom with a uniform layer of an alloy of silicon and germanium (SiGe).

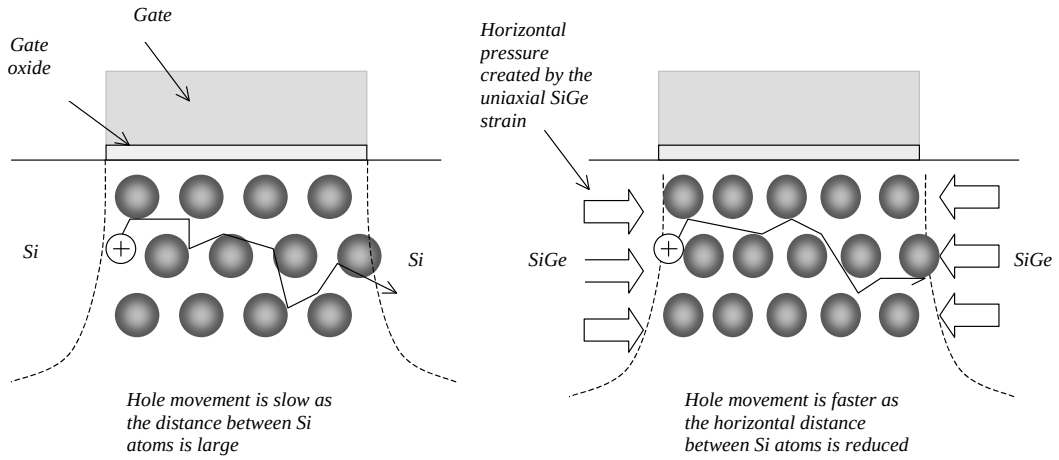


Figure 4: Compressive stain to reduce the distance between atoms underneath the gate, which speeds up the hole mobility of p-channel MOS devices

In a similar way, compressing the lattice slightly speeds up the p-type transistor, for which current carriers consist of holes. The combination of reduced channel length, decreased oxide thickness and strained silicon achieves a substantial gain in drive current for both nMOS and pMOS devices.

N-channel MOS device characteristics

The tool Microwind in its version 3.1 is configured by default in 90 nm technology. A cross-section of the n-channel and p-channel MOS devices is given in figure 5. The nMOS gate is capped with a specific silicon nitride layer that induces lateral tensile channel strain for improved electron mobility. The I/V device characteristics of the low-leakage and high-speed MOS devices listed in Table 2 are obtained using the MOS model BSIM4 (See [Sicard] for more information about this model). The device performances are close to those presented in [Ghani 90nm Intel].

Parameter	**NMOS Low leakage**	**NMOS High speed**
Drawn length	0.1µm	0.1µm
Effective length	60 nm	50 nm
Width	0.5 µm	0.5 µm
Threshold voltage	0.28	0.25
Ion (Vdd=1.2V)	0.63 mA	0.74 mA
Ioff	30 nA	300 nA

Table 2: nMOS parameters featured in the CMOS 90 nm technology provided in Microwind

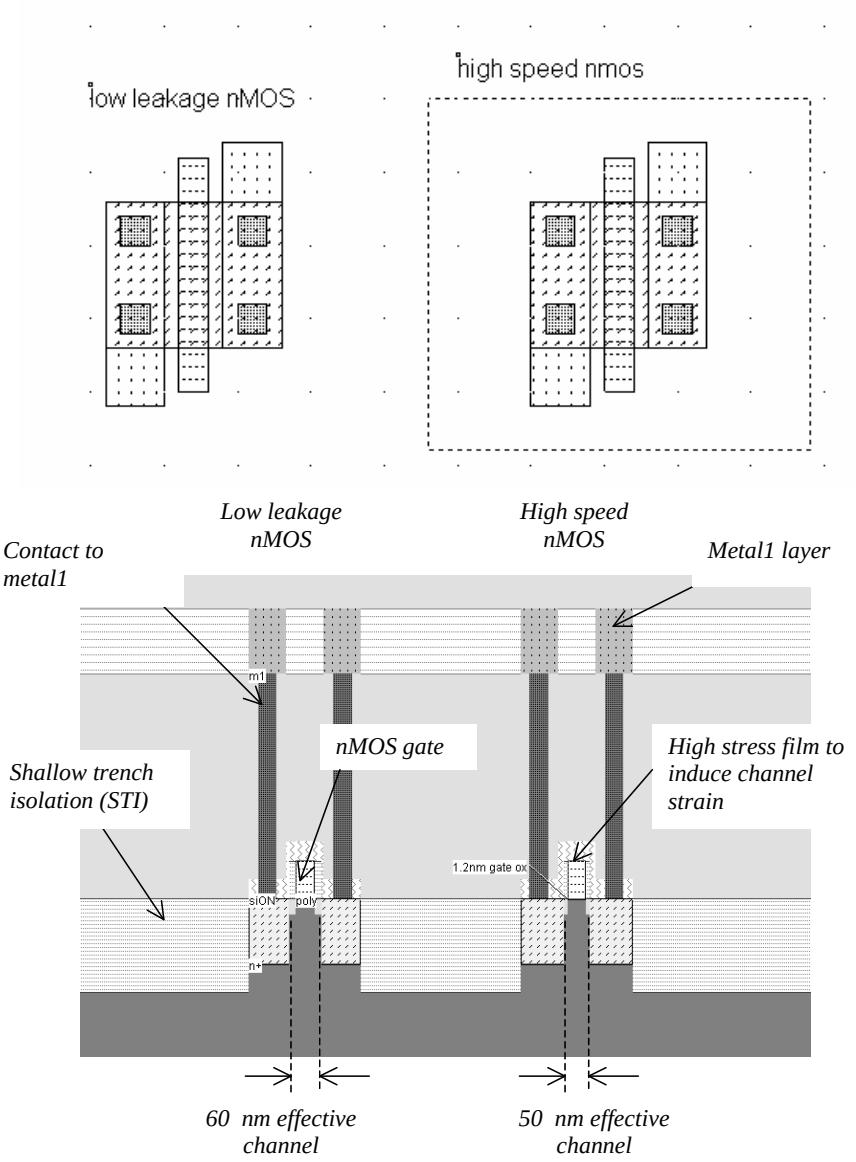
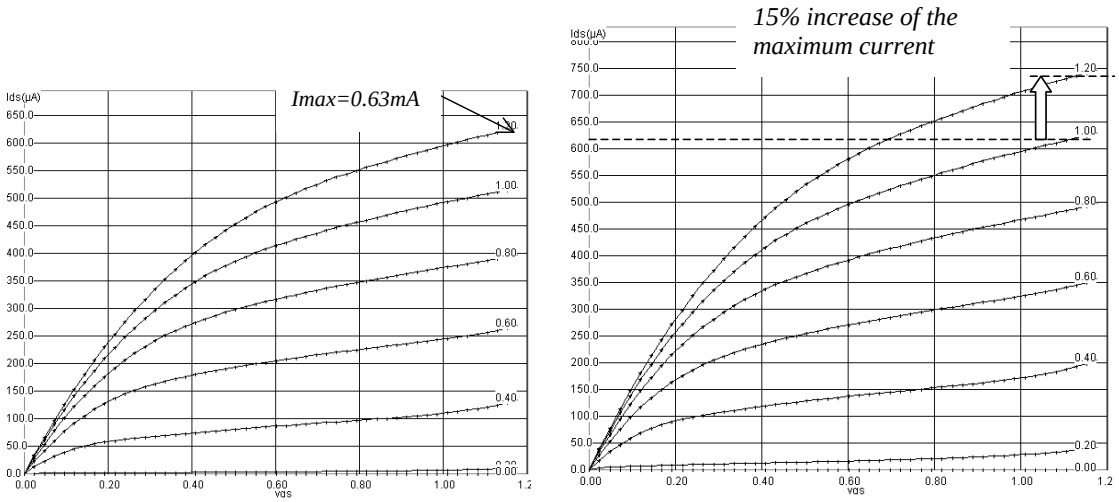


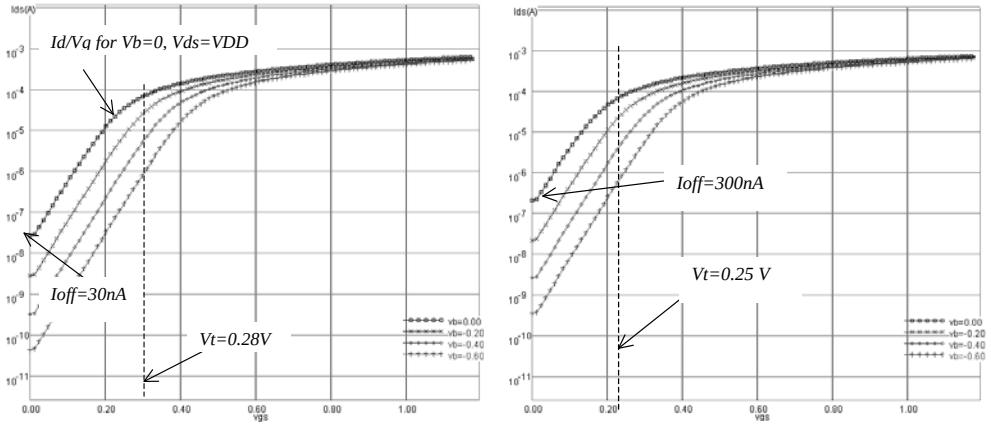
Figure 5: Bird's view and cross-section of the nMOS devices

The cross-section of the low-leakage and high-speed MOS devices do not reveal any major difference. Concerning the low-leakage MOS, the I/V characteristics reported in Fig. 6demonstrate a drive current capability around 0.6 mA for W=0.5µm, that is 1.2 mA/µm at a voltage supply of 1.2V. For the high speed MOS, the effective channel length is slightly reduced as well as the threshold voltage, to achieve an impressive drive current around 1.5 mA/µm. The drawback of this astounding current drive is the leakage current which rises from 60 nA/µm (Low leakage) to 600 nA/µm (High speed), as seen in the Id/Vg curve for Vg=0 V, Vb=0 V (Fig. 7).



(a) Low leakage *(b) High speed*

Figure 6: Id/Vd characteristics of the Low leakage and high speed nMOS devices (W=0.5µm, L=0.1µm)



(a) Low leakage *(b) High speed*

Figure 7: Id/Vgd characteristics (log scale) of the Low leakage and high-speed nMOS devices (W=0.5µm, L=0.1µm)

P-channel MOS device characteristics

The PMOS drive current in this 90 nm technology is as high as 700 µA/µm for the low-leakage MOS and up to 800 µA/µm for the high-speed MOS. These values (See table 3) are particularly high, as the target applications for this technology at Intel are high-speed digital circuits such as microprocessors. The leakage current is around 40 nA/µm for the low-leakage MOS and near 300 nA/µm for the high-speed device. The cross-section of the pMOS device reveals an SiGe material that induces compressive strain to obtain unmatched current capabilities near 1mA/µm (Fig. 8).

Parameter	pMOS Low leakage	pMOS High speed
Drawn length	0.1µm	0.1µm
Effective length	60 nm	50 nm
Width	0.5 µm	0.5 µm
Ion (Vdd=1.2V)	0.35 mA	0.39 mA
Ioff	21 nA	135 nA

Table 3: pMOS parameters featured by the 90 nm CMOS technology provided in Microwind

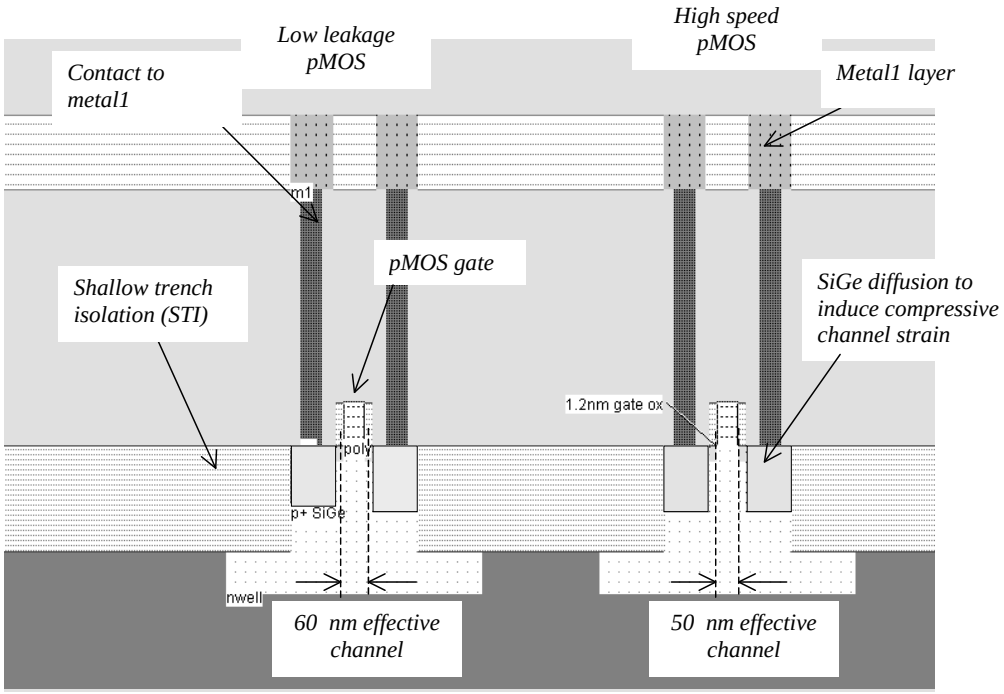


Figure 8: Cross-section of the pMOS devices

High Speed, General Purpose and Low power processes

The 90-nm process technology proposed in MICROWIND corresponds to the highest possible speed, at the price of a very important leakage current. This technology is called “High speed” as it is dedicated to application for which the highest speed is the primary objective: fast microprocessors, fast DSP, etc. The second technological option called “General Purpose” (Fig. 9) is targeted to standard products where the speed factor is not critical. The leakage current is one order of magnitude lower than for the high-speed option, with a gate delay increased by 50%, as seen in the parameters listed in Table 4. The low power option concerns integrated circuits for which the leakage must remain as low as possible, a criterion that ranks first in applications such as embedded devices, mobile phones or personal organizers. The gate delay is multiplied by 3 as compared to the high-speed option, mainly due to thicker oxides and larger gate length.

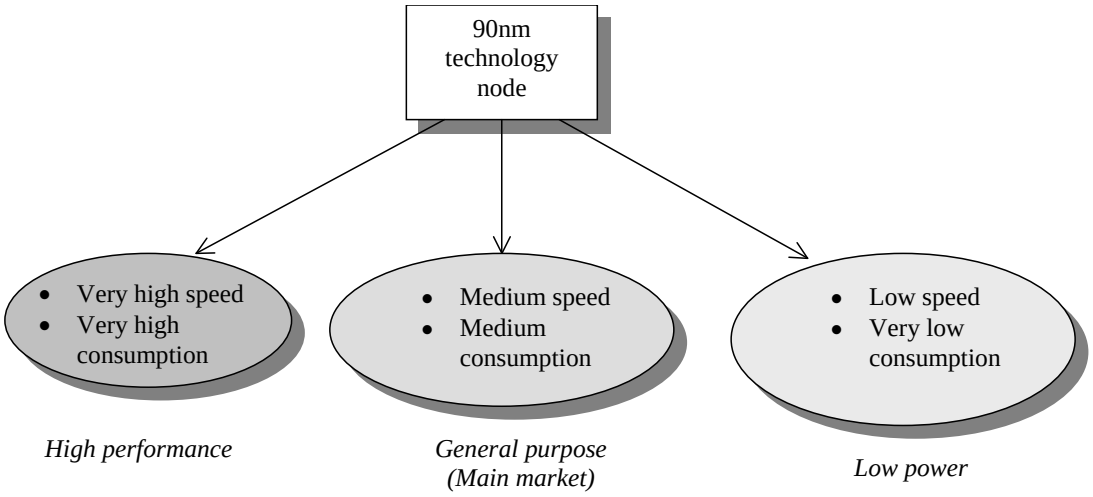


Figure 9: Introducing three variants of the 90nm technology

Technology	**High Speed**		**General Purpose**		**Low Power**	
Typical applications	Fast µP, fast DSP		ASIC, µC, FPGA		Mobiles, embedded devices	
Parameter	HS_LL	HS_HS	GP_LL	GP_HS	LP_LL	LP_HS
VCC	1.2	1.2	1.0	1.0	1.2	1.2
Tox (nm)	1.2	1.2	1.6	1.6	2.2	2.2
Leff (nm)	50	50	65	65	80	80
VT	0.28	0.25	0.35	0.25	0.50	0.40
Idsat_n (µA/µm)	1200	1500	700	800	500	600
Idsat_p (µA/µm)	700	800	300	350	200	250
Ioff (A/µm)	50n	500n	5n	50n	50p	500p
Delay (ps/stage)	7	5	12	10	25	20

Table 4: The three classes of 90 nm CMOS technologies and comparative performances

High-permittivity dielectrics

Continued thickness reduction of conventional oxides such as silicon dioxide (SiO2) results in reliability degradation and unacceptable current leakage. New dielectric materials with high permittivity (High-"K") are needed to replace SiO2, both for the MOS device itself and the embedded capacitors.

Material	**Description**	**Relative permittivity (ε_r)**	**Comments**
HfO_2	Fluor-oxide	20	Proposed for 45 nm gate oxide
Ta_2O_5	Tantalum pentoxide	25	High crystallization temperature. Reliability issues.
$Ni_xTa_2O_5$	Niobium tantalum pentoxide	28	Good candidate for MIM capacitor.
ZrO_2	Zirconium-dioxide	23	
SiO_2	Silicon dioxide	4	Important ultra-thin film leakage

Table 5: New dielectric materials than may replace SiO2 in future technologies

High capacitance passive devices (Known as Metal-Insulator-Metal, or MIM) are needed for various purposes including on-chip power supply decoupling, analog filtering for wireless applications and high-quality resonators for radio-frequency circuits. These capacitors should feature high reliability, low current leakage, low series resistance and dielectric loss, as well as being fully compatible with the standard CMOS process.

Both MOS devices and passives may benefit from high-K insulators. Concerning MOS devices, high-k dielectrics can be made thicker than SiO_2 films to obtain the same equivalent channel effect, thereby reducing leakage. Concerning passives, the larger the permittivity, the larger the charge that can be stored in memory capacitor, resulting in higher capacitance values. Alternatively, the same capacitance may require less silicon area with high-K insulators as compared to conventional SiO_2. Typical values for the capacitance range from 2 to 20 $fF/\mu m^2$.

References

[1] E. Sicard, S. Bendhia “Basic CMOS cell design”, Tata McGraw Hill, 2005

[2] T. Ghani and col. “A 90nm high volume manufacturing logic technology featuring novel 45nm gate length strained silicon CMOS transistors”, proceedings of IEDM 2003.