

Interfacing Dsch3.5 with WinSpice

Etienne SICARD
 Professor
INSA-Dgei, 135 Av de Ranguetil
31077 Toulouse – France
www.microwind.org
 email: Etienne.sicard@insa-toulouse.fr

This application note describes the interface between Dsch3.5 and the analog simulator WinSpice.

1. About WinSpice3

WinSpice3 is a general-purpose circuit simulation program for non-linear DC, non-linear transient, and linear AC analyses. A shareware version of WinSpice3 may be downloaded at web site www.winspice.com. The tool was developed by Mike Smith, OuseTech Ltd. Circuits may contain resistors, capacitors, inductors, voltage and current sources, transmission lines and semiconductor elements such as diodes and MOS devices. **WinSpice3** is based on **Spice3F4** which was developed by the Department of Electrical Engineering and Computer Sciences, University of California, Berkeley.

2. Spice Syntax

The description of basic elements used by DSCH for SPICE conversion is given in the following table.

RESISTOR RXXXXXXXX N1 N2 VALUE Example: Rvss 3 7 2ohm	N1 and N2 are the two element nodes. VALUE is the resistance (in ohms) and should be positive.
CAPACITOR CXXXXXXXX N+ N- VALUE <IC=INCOND> Example: Cb 6 2 1n	N+ and N- are the positive and negative element nodes, respectively. VALUE is the capacitance in Farads.
INDUCTOR LYYYYYYY N+ N- VALUE Example: Lvss 8 2 2n	N+ and N- are the positive and negative element nodes, respectively. VALUE is the inductance in Henry.
CURRENT SOURCE IYYYYYYY N+ N- <<DC> DC/TRAN VALUE> Example: IB 23 21 DC 0.01	N+ and N- are the positive and negative nodes, respectively. A current source of positive value forces current to flow out of the N+ node, through the source, and into the N- node. DC/TRAN is the dc and transient analysis value of the source. If the source value is zero both for dc and transient analyses, this value may be omitted. If the source value is timinvariant (e.g., a power supply), then the value may optionally be preceded by the letters DC.
Supply voltage	N+ and N- are the positive and negative nodes,

VYYYYYYY N+ N- <<DC>> DC/TRAN VALUE> Example: VDD 1 0 DC 2.0V	respectively. A voltage source of positive value is set between N+ node, and N- node.
MOS devices MXXXXXXXX ND NG NS NB MNAME <L=VAL> <W=VAL> Example: MN1 2 17 6 10 MOSN L=5U W=2U	ND, NG, NS, and NB are the drain, gate, source, and bulk (substrate) nodes, respectively. MNAME is the model name. L and W are the channel length and width, in meters.
Diode DXXXXXXXX N+ N- MNAME <AREA> <OFF> <IC=VD> <TEMP=T> Examples: DBRIDGE 2 10 DIODE1 DCLMP 3 7 DMOD 3.0 IC=0.2	N+ and N- are the positive and negative nodes, respectively.

Table 1 : basic elements in SPICE format

DSCH uses model 3 by default, however, other MOS device models may be used, which differ in the formulation of the I-V characteristic. The variable LEVEL specifies the model to be used (Table 2).

LEVEL=1	MOS1, Shichman-Hodges, very simple model
LEVEL=3	MOS3, a semi-empirical model(see [2])
LEVEL=14	BSIM4, an advanced model for deep submicron technology (see[3])

Table 2: MOS models available through DSCH and MICROWIND

.TRAN	Transient Analysis
.DC	DC Transfer Function
.AC	Small-Signal AC Analysis

Table 3: The three types of most common SPICE analysis in relation with CMOS cell simulation

Current Source Description

The current source is assigned a time-dependent value for transient analysis. There are five independent source functions: pulse, exponential, sinusoidal, piecewise-linear, and single frequency FM. In the schematic editor, the PULSE description has been implemented, as shown in figure 1.

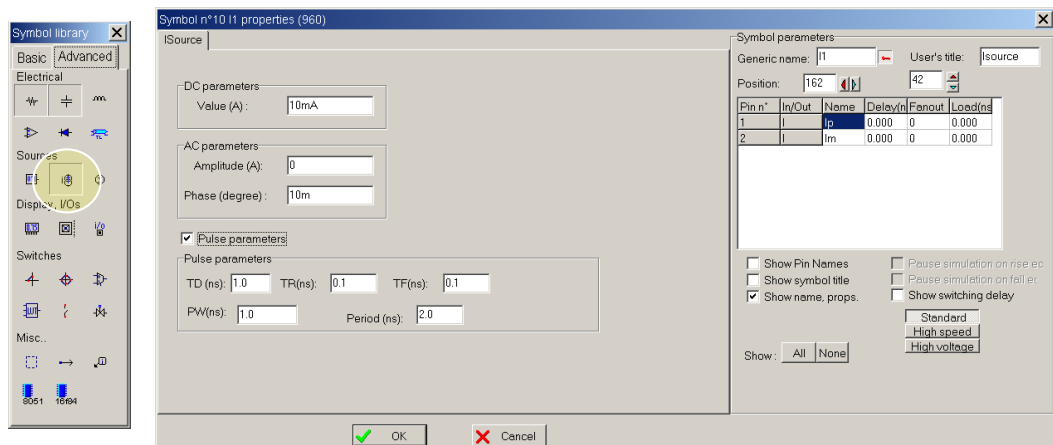


Figure 1: Current Pulse parameters in the schematic editor

The PULSE description restricts the current shape to a periodic pulse, which has a triangular shape if the pulse width parameter is set to zero (Figure 2).

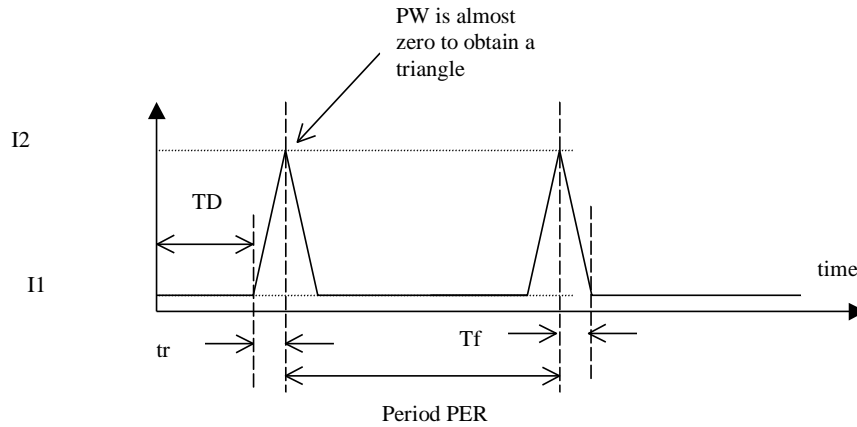


Figure 2: Current pulse parameters described as a PULSE

PULSE(I1 I2 TD TR TF PW PER)

Example: I1cpu 5 7 PULSE(0 1.2A 1.0n 2n 2n 0.1n 50n)

I1	initial value	Amps
I2	pulsed value	Amps
TD	rise time	TSTEP seconds
TF	fall time	TSTEP seconds
PW	pulse width	TSTOP seconds
PER	period	TSTOP seconds

Voltage Source Description

The voltage source is assigned a constant value to modelize the supply source. In figure 3, the voltage source is constant, with a DC value of 1 V.

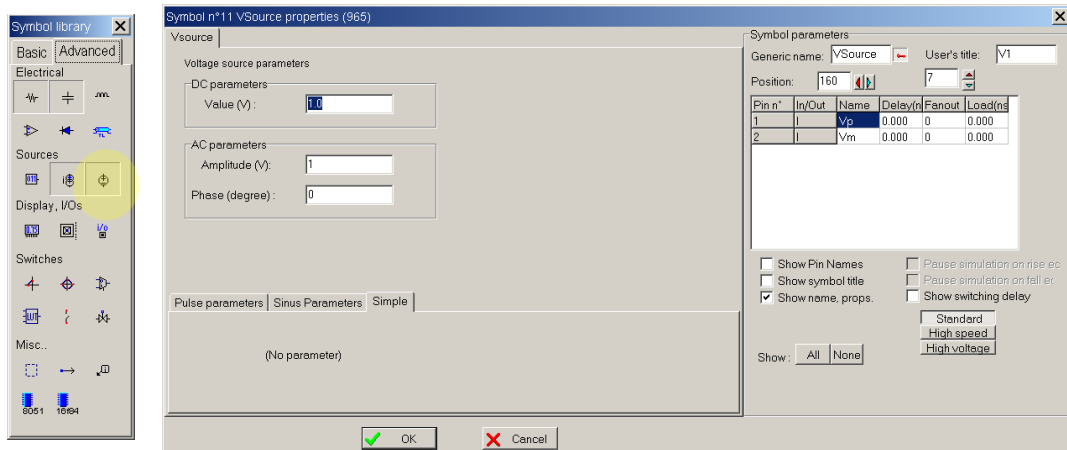


Figure 3: Constant voltage source

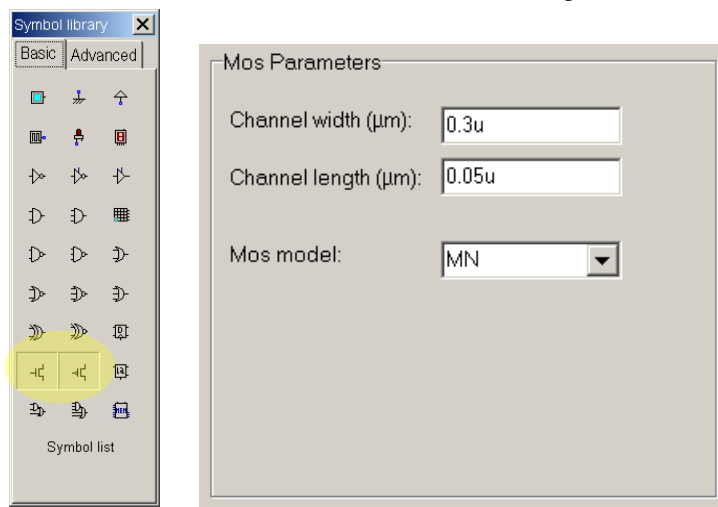


Figure 4: MOS parameters

MOS Models

When instantiating a MOS symbol, DSCH 3.5 adds the contents of the file “spice.lib” in the SPICE text. The text included in “spice.lib” is a SPICE compatible-text which contains the model parameters. By default, DSCH 3.5 is configured in 45-nm CMOS technology. By default, the “MN” and “MP” models refer to 45-nm MOS parameters, as may be found in “spice.lib” (Fig. 4). Notice that the default size (Width and Length) is also dependent on the technology. The default length in 45-nm technology is 0.05 μm (50 nm), and the default width is

```
*---MOS-----
* Defaul Mos models : corresponds to 45nm 1V
* Generated from Microwind 45nm
* Ref: 45nm application note www.microwind.org
*
* Mos models in 45nm
* n-MOS Model 3 :
.MODEL MN NMOS LEVEL=3 VTO=0.18 UO=160.000 TOX= 3.5E-9
+LD =0.005U THETA=0.300 GAMMA=0.400
+PHI=0.150 KAPPA=0.350 VMAX=180.00K
+CGSO=100.0p CGDO=100.0p
+CGBO= 60.0p CJSW=240.0p
*
* p-MOS Model 3:
.MODEL MP PMOS LEVEL=3 VTO=-0.15 UO=120.000 TOX= 3.5E-9
+LD =0.005U THETA=0.300 GAMMA=0.400
+PHI=0.150 KAPPA=0.350 VMAX=180.00K
+CGSO=100.0p CGDO=100.0p
+CGBO= 60.0p CJSW=240.0p
*
```

DSCH uses “LEVEL=3” by default. The variable LEVEL specifies the model to be used (Table 2). Note that Microwind uses BSIM4, an advanced model for deep submicron technology (see[3]).

Type of Analysis

There are mainly three analysis of interest that are listed below. Other types of analysis exist in WinSpice as described in [1], which are not introduced in this appendix.

.AC: Small-Signal AC Analysis

General form:

```
.AC DEC ND FSTART FSTOP
.AC LIN NP FSTART FSTOP
```

Examples:

```
.AC DEC 10 1K 100MEG
.AC LIN 100 1MEG 10G
```

DEC stands for decade variation, and ND is the number of points per decade. OCT stands for octave variation, and NO is the number of points per octave. LIN stands for linear variation, and NP is the number of points. FSTART is the starting frequency, and FSTOP is the final frequency.

.DC: DC Transfer Function

General form:

```
.DC SRCNAM VSTART VSTOP VINCR [SRC2 START2 STOP2 INCR2]
```

Examples:

```
.DC VIN 0.25 5.0 0.25
.DC VDS 0 10 .5 VGS 0 5 1
```

The DC line defines the DC transfer curve source and sweep limits (again with capacitors open and inductors shorted). SRCNAM is the name of an independent voltage or current source. VSTART, VSTOP, and VINCR are the starting, final, and incrementing values respectively.

The first example causes the value of the voltage source VIN to be swept from 0.25 Volts to 5.0 Volts in increments of 0.25 Volts. A second source (SRC2) may optionally be specified with associated sweep parameters. In this case, the first source is swept over its range for each value of the second source. This option can be useful for obtaining semiconductor device output characteristics.

.TRAN: Transient Analysis

General form:

```
.TRAN TSTEP TSTOP <UIC>
```

Example:

```
.TRAN 1NS 1000NS
```

TSTEP is the printing or plotting increment for line printer output. TSTOP is the final time. The transient analysis always begins at time zero.

3. Generate a SPICE file from Schematics**Transient Simulation**

Not all symbols may be translated into Spice. Only R,L,C elements, transmission lines, current sources, voltage sources, MOS and diode devices may be translated and simulated. Logic gates such as AND, NAND, NOR, XOR, etc. cannot be converted into Spice. The only possibility is to replace the gates by their MOS-based equivalent circuits, as explained in chapter 4 of the book "Basic CMOS cell design" [4].

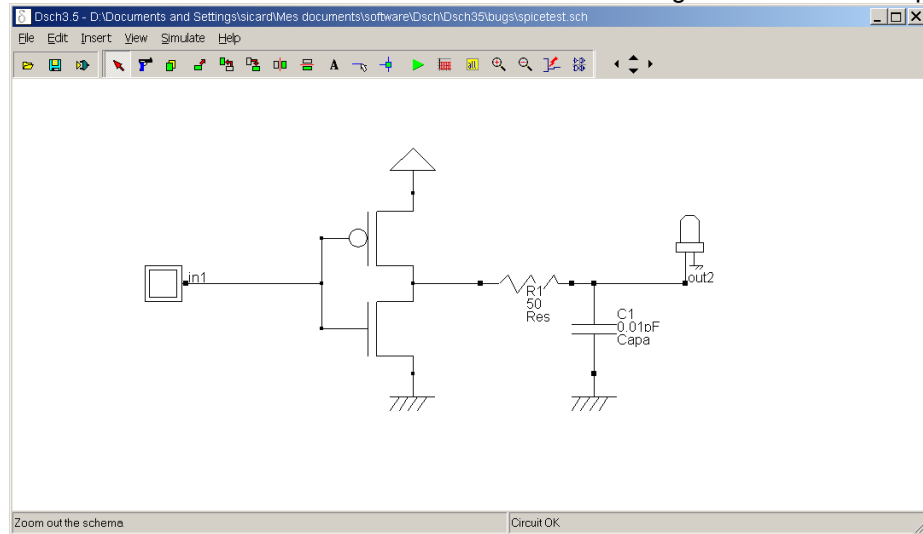


Figure 5: A CMOS inverter example (spice/spiceinv.sch)

Let us consider the schematic diagram of figure 5, containing one nMOS, one pMOS, VSS and VDD supplies and an RC circuit. This corresponds to an inverter connected to a load. The button is necessary to declare the input, the light is mandatory to declare the output. Invoke the command **File** → **Generate Spice file** or click <Ctrl>+<G>. A screen appears (figure 5).

The text is saved using the same project name, with the appendix <.CIR>. In figure 6, the text file starts with comments (*, *' in the first column), the declaration of voltage sources (,V' as the first character), the R,L,C components (here one capacitor C1 and one resistor R1), the active devices (one pMOS, one nMOS) and the simulation control.

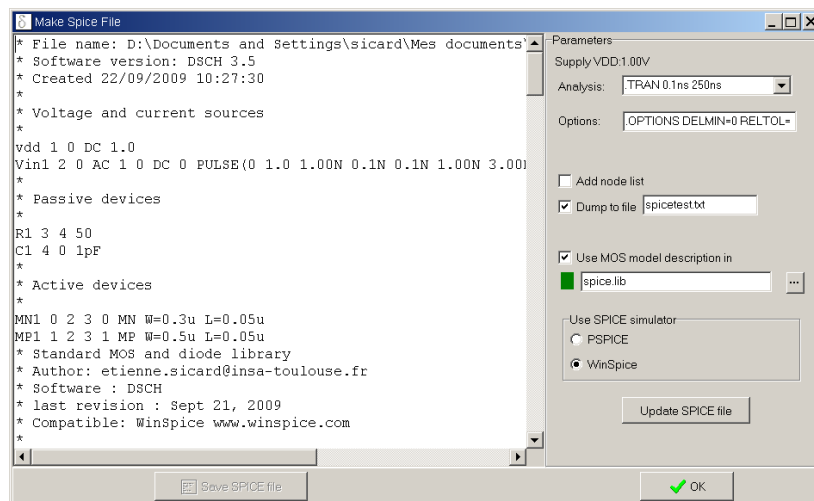


Figure 6: The SPICE file generated from the schematic diagram (spice/spiceinv.sch)

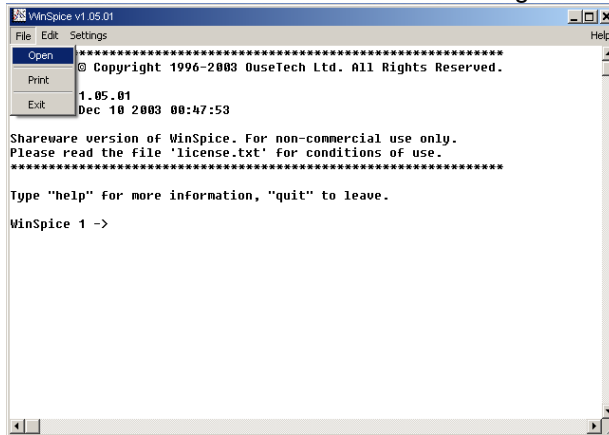


Figure 7: The WinSpice initial screen

Run WinSPICE Simulation

Start the WinSpice program, and click **File** → **Open** (figure 7). Select the desired .CIR file. In our example, the file generated by DSCH is "spiceInv.CIR". The simulation is performed in time domain, and the following screen appears. The .TRAN analysis is conducted during 100NS. The result is stored in a file called "spiceInv.txt". The plot of the transient simulation appears in a new window reported in figure 8. Using the mouse, define an area to zoom at, the corresponding zone is displayed in a new window.

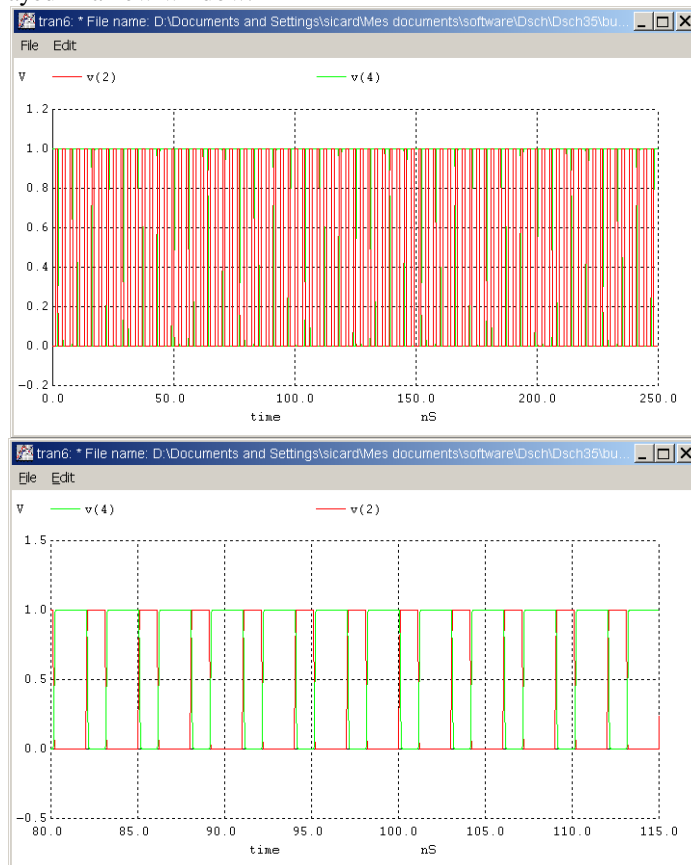


Figure 8: The transient simulation of the inverter (spice/spiceinv.sch)

Defining the type of Analysis

By default, the analysis is the time-domain transient simulation “.TRAN”. The duration of the simulation is 250 ns by default. The text added in the layout starting by “.TRAN” (“.TRAN 0.1N 100N” in the case of figure 9) is recognized by the SPICE translator as the new transient simulation control. Three keywords are recognized by DSCH3.5 :

- “.TRAN xxx”
- “.DC xxx”
- “.AC xxx”

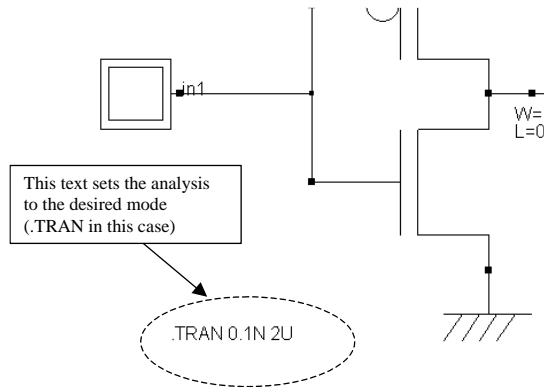


Figure 9: Defining the analysis parameters by adding a label in the schematic diagram

Input/outputs

All clocks, keyboard, leds and displays are declared as voltage outputs. In the case of the inverter, the input “IN1” and the output “OUT2” appear in the “plot” control line as voltage V(2) and V(4).

Control line	Description
.TRAN 0.1N 100N	Transient analysis, step 0.1N, duration 100ns
.control	Start the control section
Run	Run the transient analysis
set nobreak	No break in the output text file
print V(2) V(4) > spiceInv.txt	Dump two voltages in the file "spiceInv.txt"
plot V(2) V(4)	Open a window and plot the same voltages
.endc	End of control section
.OPTIONS DELMIN=0 RELTOL=16	Options for simulation
.END	End of SPICE file

Table 4: Control section at the end of the SPICE file

DC Analysis

The example proposed in figure 8 corresponds to the transfer function of the output voltage versus the input voltage. The script of the SPICE control (text included in the schematic diagram) is modified manually so that the “TRAN” analysis is replaced by the “DC” analysis. The DC parameters are the control node (Here *Vin*), the start voltage (0.0 V), the stop voltage (1.0 V) and the voltage step (10 mV). The WINSPICE result shows that the inverter switches when *Vin*=0.55V.

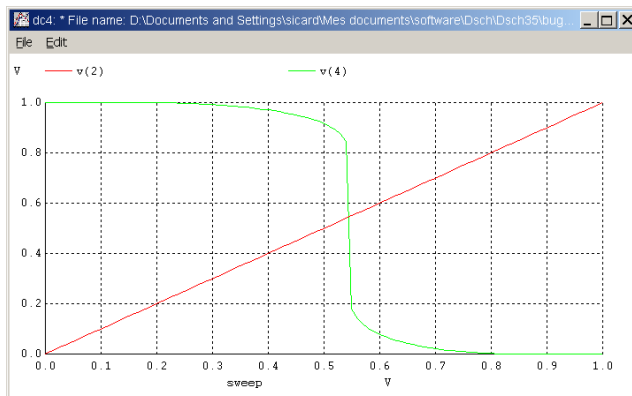
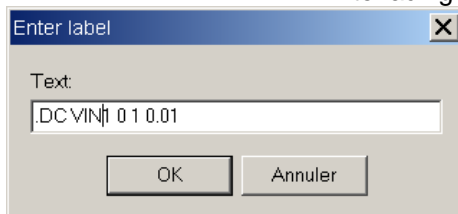


Figure 10: the transfer characteristics of the inverter using DC simulation (spice/spiceinvdc.sch)

```
.control
dc Vin1 0 1.0 0.01
print V(2) V(4) > out.txt
plot V(2) V(4)
.endc
```

Frequency Analysis

An example of frequency simulation using WINSPICE is proposed in this paragraph. The goal of the frequency analysis is to find out the cut-off frequency of an amplifier. We start from the schematic diagram of a MOS connected as an amplifier, loaded by a 0.01 pF capacitor at its output (Figure 11). An AC simulation can be performed by declaring an AC source. The proposed analysis covers the frequency range from 1 MHz to 10 GHz by decades (“DEC”, 10 points per decade). The corresponding control line is « .AC DEC 10 1MEG 10G ».

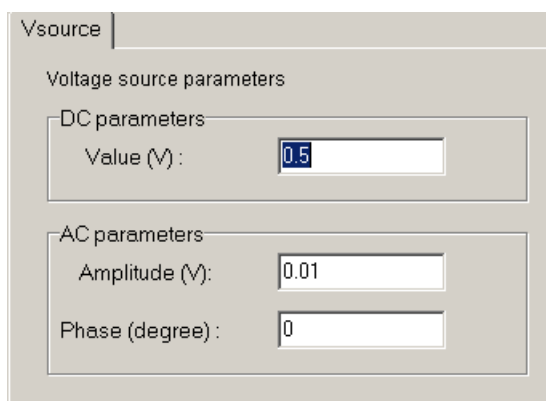


Figure 11: the voltage source is configured for AC analysis. Note that the DC value is also taken into account for the AC analysis (spice/spiceampliac.sch)

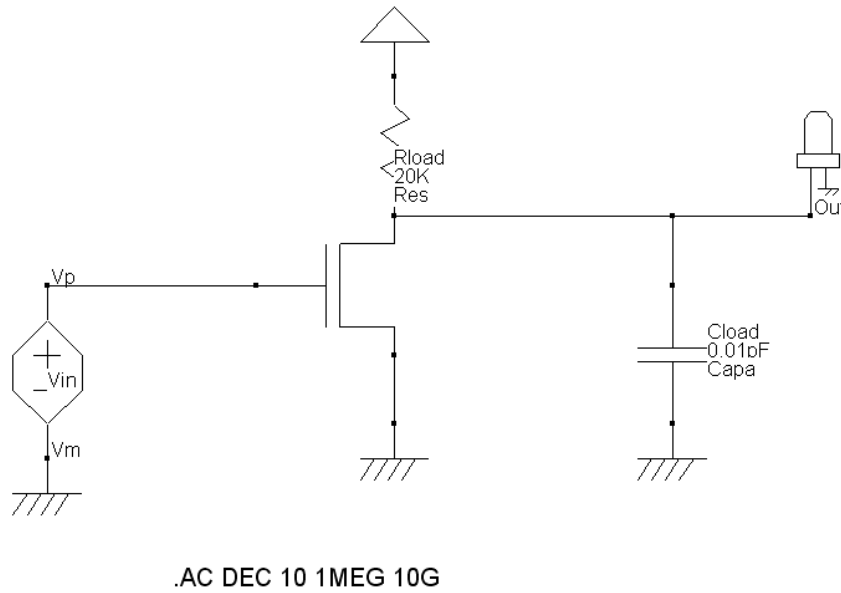


Figure 12: the MOS amplifier used for AC analysis, and the text controlling the AC simulation (spice/spiceampliac.sch)

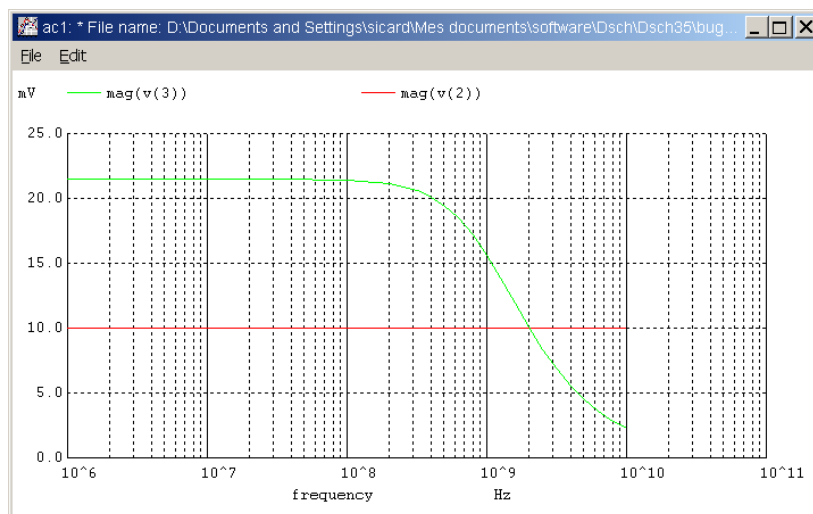


Figure 13: the MOS amplifier used for AC analysis, and the text controlling the AC simulation (spice/spiceampliac.sch)

The simulation result is plotted in Fig. 13. The X Axis is in log scale, due to the declaration of « DEC » in the AC command line. The magnitude of the output is in green. We see the amplification effect as the output is 2 times larger than the input (10 mV defined in the AC parameters), until 1 GHz.

The usual plot unit for the output voltage is the decibel, as given in equation 1.

$$VdB = 20 \log(V) \quad (\text{Eq. 1})$$

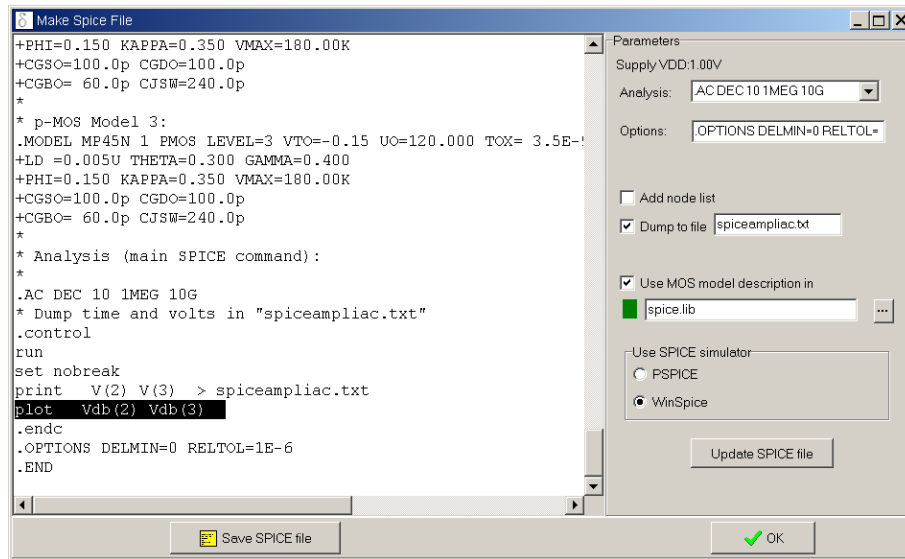


Figure 14: Modifying the SPICE text to plot the result in dB (spice/spiceampliac.sch)

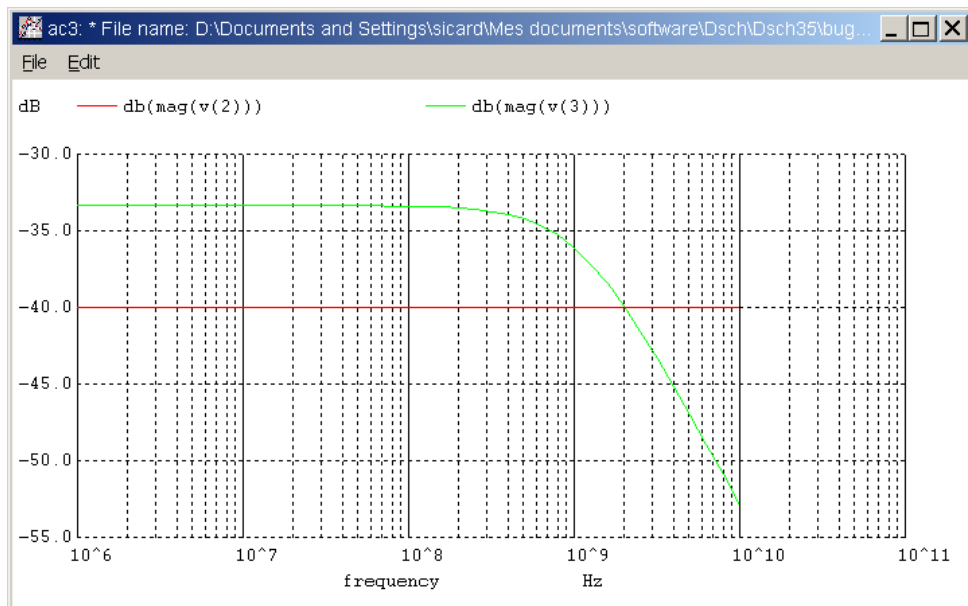


Figure 15: Voltages plotted in dB (spice/spiceampliac.sch)

To plot the output directly in dB, the SPICE text should be modified manually in the SPICE window as detailed in Fig. 15. Change V(2) into Vdb(2), and V(3) into Vdb(3). Click « Save SPICE File », the new plot appears in Fig. xxx. Note that -40 dB corresponds to 0.01 V (0 dB = 1V, -20 dB = 100 mV, etc.).

References

- [1] WinSpice3 User's Manual, October 2003, Mike Smith, www.winspice.com
- [2] A. Vladimirescu and S. Liu, The Simulation of MOS Integrated Circuits Using SPICE2, ERL Memo No. ERL M80/7, Electronics Research Laboratory, University of California, Berkeley, October 1980

4. Appendix A – MOS & Diode Model Library

```

* Standard MOS and diode library
* Author: etienne.sicard@insa-toulouse.fr
* Software : DSCH
* last revision : Sept 21, 2009
* Compatible: WinSpice www.winspice.com
*
* Note: Dsch will use "MN" and "MP" default calls for Mos devices
* "DIOD" for diodes and "CLAMP" for clamp diodes
* Note: other MOS models are provided for several technologies
*
*---Diodes-----
* Simple diode
.MODEL DIOD D RS=5 BV=15 N=1.0
*
* Clamp diode
.MODEL CLAMP D RS=2 BV=10 N=1.2
*
*---Capa model-----
* Add a first order temperature influence through TC1
.MODEL CMODEL CAP(TC1=-0.001)
*
*---MOS-----
* Defaul Mos models : corresponds to 45nm 1V
* Generated from Microwind 45nm
* Ref: 45nm application note www.microwind.org
*
* Mos models in 45nm
* n-MOS Model 3 :
.MODEL MN NMOS LEVEL=3 VTO=0.18 UO=160.000 TOX= 3.5E-9
+LD =0.005U THETA=0.300 GAMMA=0.400
+PHI=0.150 KAPPA=0.350 VMAX=180.00K
+CGSO=100.0p CGDO=100.0p
+CGBO= 60.0p CJSW=240.0p
*
* p-MOS Model 3:
.MODEL MP PMOS LEVEL=3 VTO=-0.15 UO=120.000 TOX= 3.5E-9
+LD =0.005U THETA=0.300 GAMMA=0.400
+PHI=0.150 KAPPA=0.350 VMAX=180.00K
+CGSO=100.0p CGDO=100.0p
+CGBO= 60.0p CJSW=240.0p
*
* Mos models in 0.35µm
* Model 3 n-channel MOS
.MODEL MN035 NMOS
+ LEVEL=3          TPG=+1
+ GAMMA=0.2        THETA=0.5          KAPPA=0.1          ETA=0.002
+ DELTA=0.0        UO=620            VMAX=100E3        VTO=0.5
+ TOX=5e-9         XJ=0.1U          LD=0.00U          NSUB=1E+18
+ NSS=0.2          NFS=7E11         RD=1              RS=1
+ CJ=4.091E-4      MJ=0.307         PB=1.0
+ CJSW=3.078E-10  MJSW=1.0E-2
+ CGSO=3.93E-10   CGDO=3.93E-10
* Model 3 p-channel MOS
.MODEL MP035 PMOS
+ LEVEL=3          TPG=-1
+ GAMMA=0.2        THETA=0.5          KAPPA=0.01        ETA=0.001

```

DSCH APPLICATION NOTE

Interfacing DSCH 3.5 to WinSpice

```

+ DELTA=0.0          UO=250          VMAX=100E3        VTO=-0.5
+ TOX=5E-9           XJ=0.1U         LD=0.0U           NSUB=1E+18
+ NSS=0.0            NFS=7E11         RD=1              RS=1
+ CJ=6.852E-4        MJ=0.429        PB=1.0
+ CJSW=5.217E-10    MJSW=0.351
+ CGSO=7.29E-10     CGDO=7.29E-10
*
* Model 3 n-channel MOS
.MODEL MN035 NMOS
+ LEVEL=3            TPG=+1
+ GAMMA=0.2          THETA=0.5        KAPPA=0.1         ETA=0.002
+ DELTA=0.0          UO=620           VMAX=100E3        VTO=0.5
+ TOX=5e-9           XJ=0.1U         LD=0.00U         NSUB=1E+18
+ NSS=0.2            NFS=7E11         RD=1              RS=1
+ CJ=4.091E-4        MJ=0.307        PB=1.0
+ CJSW=3.078E-10    MJSW=1.0E-2
+ CGSO=3.93E-10     CGDO=3.93E-10
* Model 3 p-channel MOS
.MODEL MP035 PMOS
+ LEVEL=3            TPG=-1
+ GAMMA=0.2          THETA=0.5        KAPPA=0.01        ETA=0.001
+ DELTA=0.0          UO=250           VMAX=100E3        VTO=-0.5
+ TOX=5E-9           XJ=0.1U         LD=0.0U           NSUB=1E+18
+ NSS=0.0            NFS=7E11         RD=1              RS=1
+ CJ=6.852E-4        MJ=0.429        PB=1.0
+ CJSW=5.217E-10    MJSW=0.351
+ CGSO=7.29E-10     CGDO=7.29E-10
*
* Mos models in 0.25µm
* Model 3 n-channel MOS
.MODEL MN025 NMOS
+ LEVEL=3            TPG=+1
+ GAMMA=0.2          THETA=0.5        KAPPA=0.1         ETA=0.002
+ DELTA=0.0          UO=620           VMAX=100E3        VTO=0.4
+ TOX=3e-9           XJ=0.1U         LD=0.00U         NSUB=1E+18
+ NSS=0.2            NFS=7E11         RD=1              RS=1
+ CJ=4.091E-4        MJ=0.307        PB=1.0
+ CJSW=3.078E-10    MJSW=1.0E-2
+ CGSO=3.93E-10     CGDO=3.93E-10
* Model 3 p-channel MOS
.MODEL MP025 PMOS
+ LEVEL=3            TPG=-1
+ GAMMA=0.2          THETA=0.5        KAPPA=0.01        ETA=0.001
+ DELTA=0.0          UO=250           VMAX=300E3        VTO=-0.4
+ TOX=3E-9           XJ=0.1U         LD=0.0U           NSUB=1E+18
+ NSS=0.0            NFS=7E11         RD=1              RS=1
+ CJ=6.852E-4        MJ=0.429        PB=1.0
+ CJSW=5.217E-10    MJSW=0.351
+ CGSO=7.29E-10     CGDO=7.29E-10
*
* Mos models in 0.12µm
* Model 3 n-channel MOS
.MODEL MN012 NMOS
+ LEVEL=3            TPG=+1
+ GAMMA=0.2          THETA=0.5        KAPPA=0.1         ETA=0.002
+ DELTA=0.0          UO=620           VMAX=100E3        VTO=0.35
+ TOX=2e-9           XJ=0.1U         LD=0.00U         NSUB=1E+18
+ NSS=0.2            NFS=7E11         RD=1              RS=1
+ CJ=4.091E-4        MJ=0.307        PB=1.0
+ CJSW=3.078E-10    MJSW=1.0E-2
+ CGSO=3.93E-10     CGDO=3.93E-10
* Model 3 p-channel MOS
.MODEL MP012 PMOS
+ LEVEL=3            TPG=-1
+ GAMMA=0.2          THETA=0.5        KAPPA=0.01        ETA=0.001
+ DELTA=0.0          UO=250           VMAX=300E3        VTO=-0.35
+ TOX=2E-9           XJ=0.1U         LD=0.0U           NSUB=1E+18
+ NSS=0.0            NFS=7E11         RD=1              RS=1
+ CJ=6.852E-4        MJ=0.429        PB=1.0
+ CJSW=5.217E-10    MJSW=0.351

```

```
+ CGSO=7.29E-10      CGDO=7.29E-10
*
*
* Mos models in 90nm
* n-MOS Model 3 :
.MODEL MN90N NMOS LEVEL=3 VTO=0.34 UO=350.000 TOX= 1.2E-9
+LD =0.020U THETA=0.890 GAMMA=0.500
+PHI=0.150 KAPPA=0.130 VMAX=125.00K
+CGSO=100.0p CGDO=100.0p
+CGBO= 60.0p CJSW=240.0p
*
* p-MOS Model 3:
* low leakage
.MODEL MP90N PMOS LEVEL=3 VTO=-0.32 UO=120.000 TOX= 1.2E-9
+LD =0.020U THETA=1.800 GAMMA=0.400
+PHI=0.150 KAPPA=0.310 VMAX=90.00K
+CGSO=100.0p CGDO=100.0p
+CGBO= 60.0p CJSW=240.0p
*
*
* Mos models in 65nm
* n-MOS Model 3 :
* low leakage
.MODEL MN65N NMOS LEVEL=3 VTO=0.34 UO=300.000 TOX= 1.1E-9
+LD =0.010U THETA=0.890 GAMMA=0.500
+PHI=0.150 KAPPA=0.130 VMAX=125.00K
+CGSO=100.0p CGDO=100.0p
+CGBO= 60.0p CJSW=240.0p
*
* p-MOS Model 3:
* low leakage
.MODEL MP65N PMOS LEVEL=3 VTO=-0.32 UO=110.000 TOX= 1.1E-9
+LD =0.020U THETA=1.800 GAMMA=0.400
+PHI=0.150 KAPPA=0.310 VMAX=90.00K
+CGSO=100.0p CGDO=100.0p
+CGBO= 60.0p CJSW=240.0p
*
*
* Mos models in 45nm
* n-MOS Model 3 :
.MODEL MN45N NMOS LEVEL=3 VTO=0.18 UO=160.000 TOX= 3.5E-9
+LD =0.005U THETA=0.300 GAMMA=0.400
+PHI=0.150 KAPPA=0.350 VMAX=180.00K
+CGSO=100.0p CGDO=100.0p
+CGBO= 60.0p CJSW=240.0p
*
* p-MOS Model 3:
.MODEL MP45N 1 PMOS LEVEL=3 VTO=-0.15 UO=120.000 TOX= 3.5E-9
+LD =0.005U THETA=0.300 GAMMA=0.400
+PHI=0.150 KAPPA=0.350 VMAX=180.00K
+CGSO=100.0p CGDO=100.0p
+CGBO= 60.0p CJSW=240.0p
```