XOR GATE DESIGN IN 14-NM FINFET TECHNOLOGY

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This application note discusses the implementation of the XOR/XNOR gates in nano-CMOS technologies. The limitations of the 6T-design are detailed, and two versions of the XOR gate in 16-transistor and 10-Transistor versions are discussed.

6T-XOR GATE DESIGN

The 6-transistor XOR gate design is a very compact solution for implementing the XOR function. The schematic diagram is shown in Figure 1. The main drawback is the use of pass transistors which may create non-ideal logic levels due to threshold voltage degradation. In short, n-channel transistors cannot transfer the level 1 correctly, the p-channel transistors cannot transfer the level 0 correctly. Other values are correctly executed. Using DSCH, the observed simulation is always correct, as DSCH do not take into account "weak-1" and "weak-0" levels.

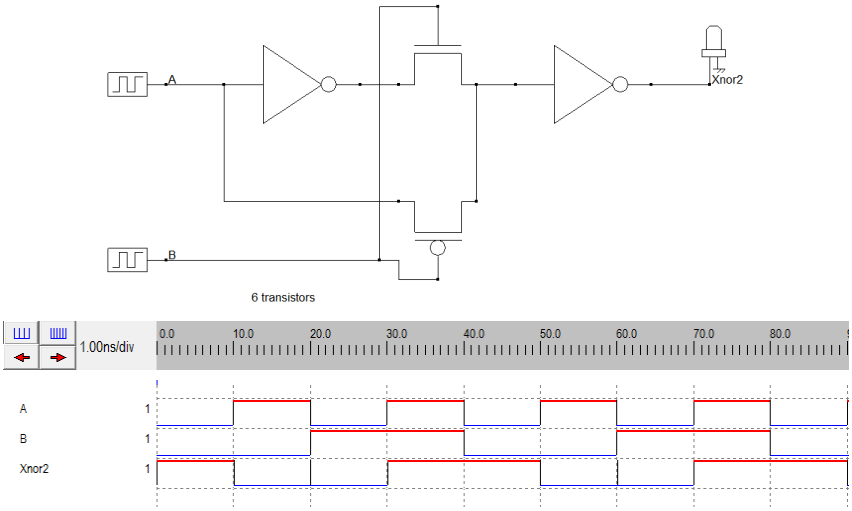


Figure 1: schematic diagram and logic simulation of the 2-input XNOR gate

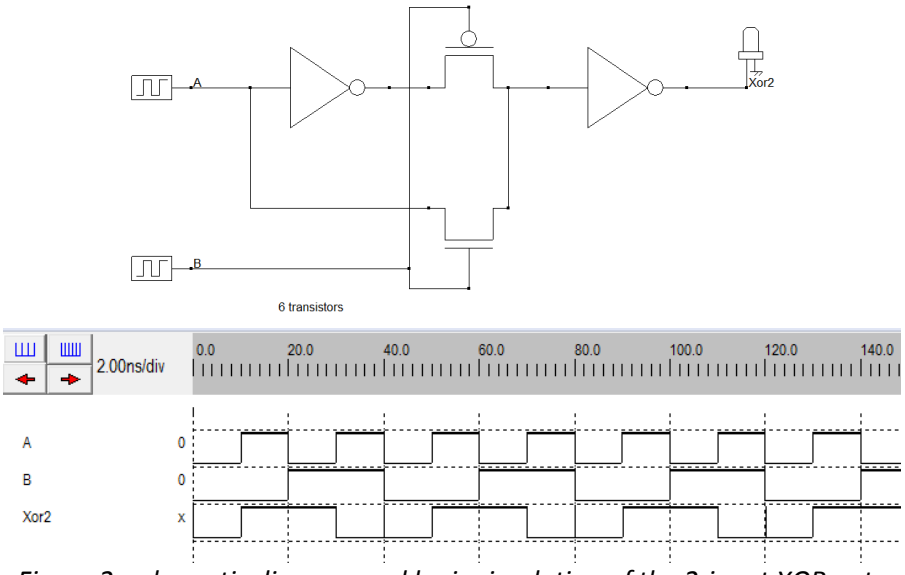
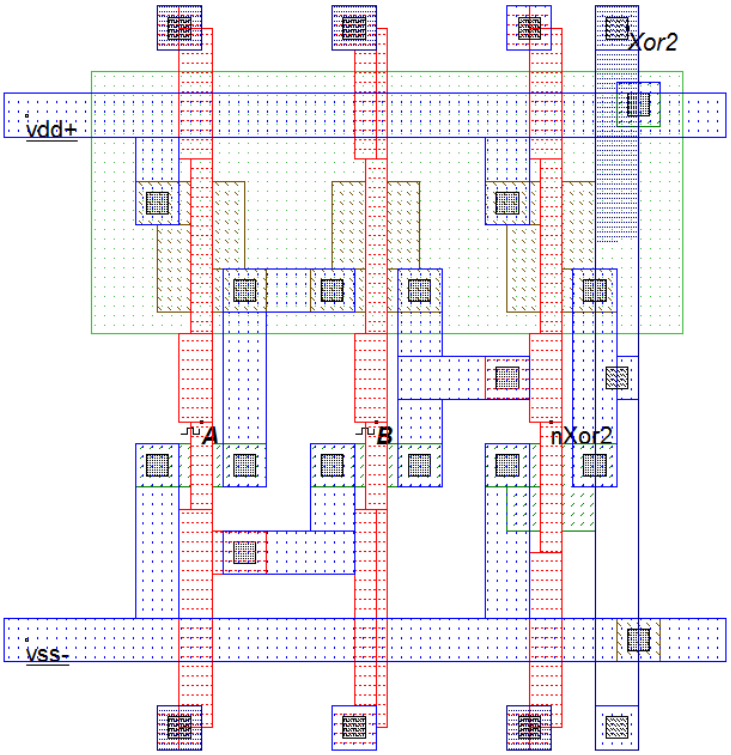


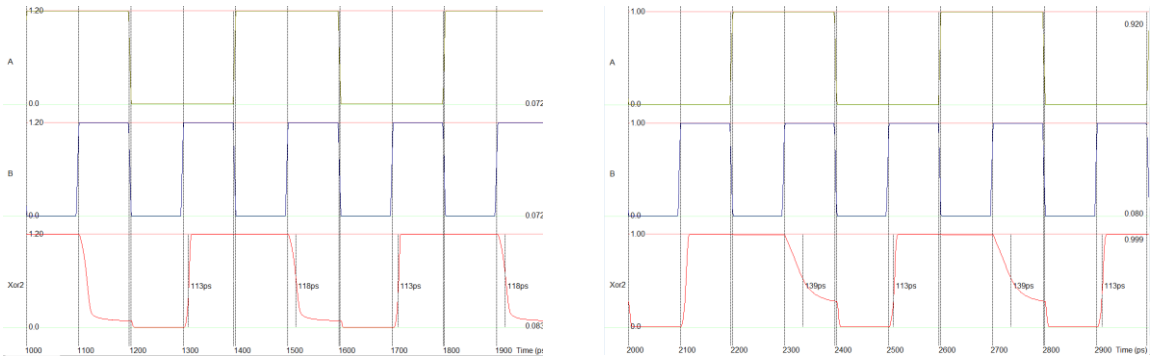
Figure 2: schematic diagram and logic simulation of the 2-input XOR gate

The compilation of the XOR gate using Microwind leads to a compact layout, but the non-ideal internal levels do not induce a correct inverter simulation, which creates important negative effects:

- Very large delays
- Important static consumption

These effects can be partially tolerated in sub-micron technologies down to 90-nm node. However, the effects tend to worsen with the technology scale down. In 20-nm, the XOR introduces very long delays and incorrect levels (Fig. 3).





(a) 90-nm CMOS: long delays and imperfect levels

(b) 20-nm simulation: very long delays and incorrect levels

Figure 3: MosFET Implementation and simulation of the 6-transistor version of the 2-input XOR gate

16-T XOR Gate

A straightforward approach for XOR design is to implement 2 inverters and 3 NAND2 gates to build the appropriate function. The result is a clean signal put the delay may consist of 1 invert and 3 chained NAND gates that is 4 stages.

$$XOR = A\bar{B} + B\bar{A} = \overline{A\bar{B}} \times \overline{B\bar{A}}$$

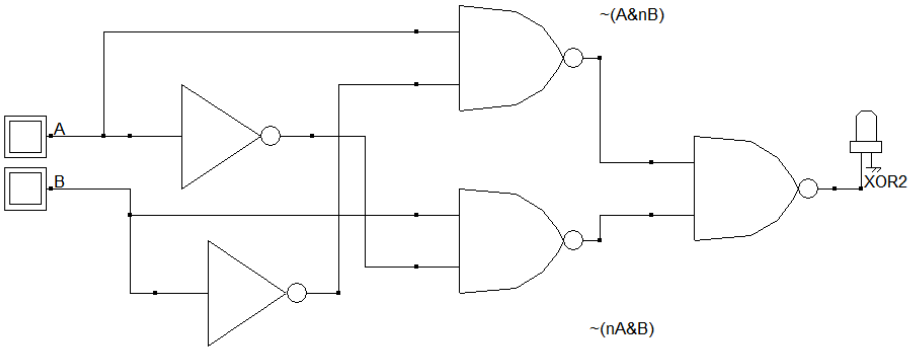


Figure 4: Schematic diagram of the 16-transistor version of the 2-input XOR gate

The 16-Transistor implementation of the XOR2 is used for VERILOG compilation into layout. Figure 5 shows the resulting layout with two inverters on the left side, 3 gates on the right side. The simulations shows a worst-case delay around 7 ps in 14-nm technology, with a fanout of 1 and around 3µm of interconnects.

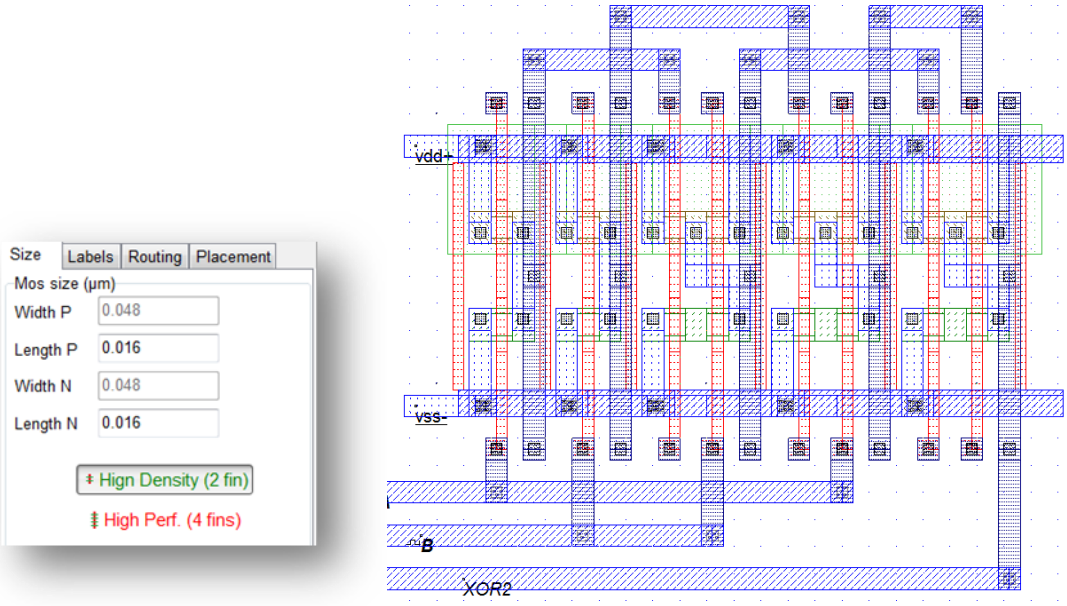


Figure 5: Compilation of the XOR symbol into 16-FinFET XOR gate (2 fins)

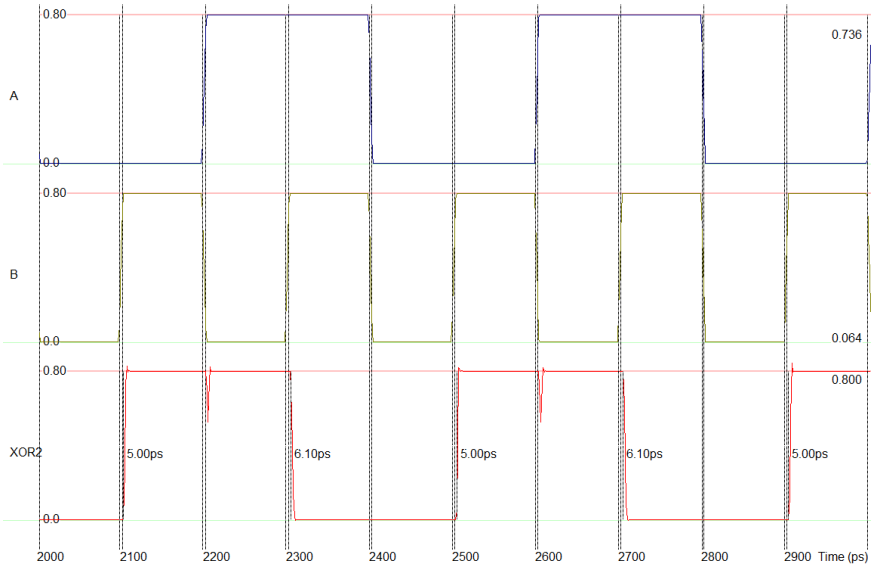


Figure 6: Simulation of the XOR symbol into 16-transistor XOR gate

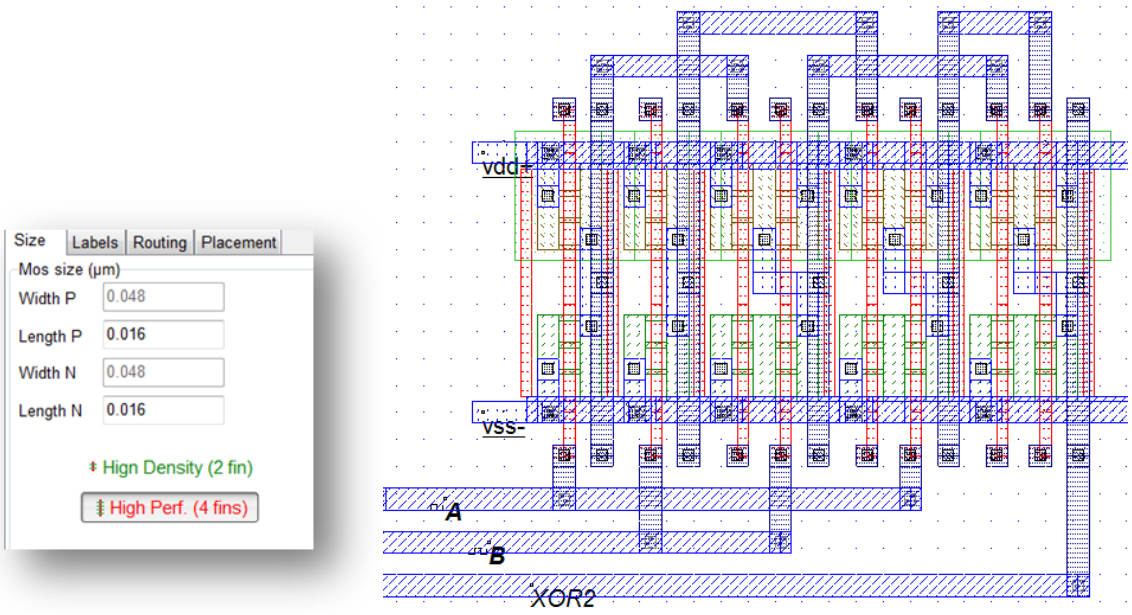


Figure 7: Compilation of the XOR into 16nm -FinFET XOR gate (4 fins)

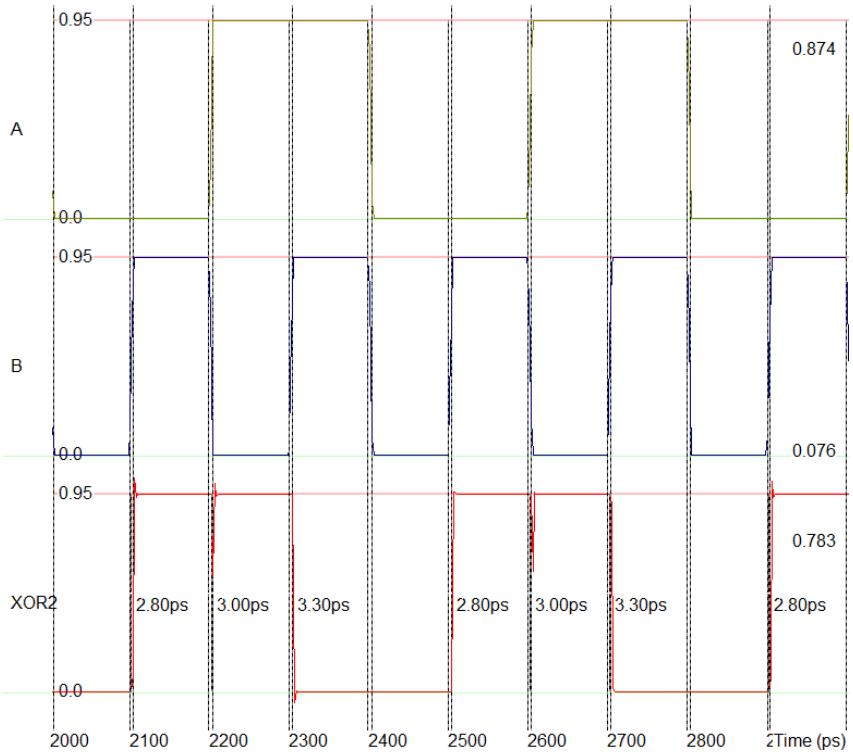


Figure 8: Simulation of the XOR in FireStarter mode

The Firestarter mode consist in putting the circuit in maximum speed conditions. This is obtained with High speed option, 4 fins and a supplementary boost of VDD supply from 0.8 to 0.95V. The switching speed is reduced to 3.3 ps (a factor of 2 as compared to 2-Fin nominal VDD and low leakage option). However, the power consumption is severely increased.

10-T XOR Gate

The original 6-T schematics can be re-arranged by replacing the dangerous pass single transistors by safe transmission gates. This requires to produce nB using a supplementary inverter. The schematics is reported in Figure 7.

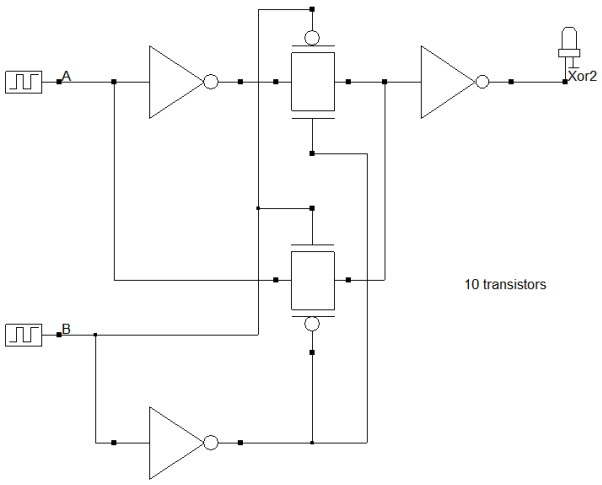


Figure 7: Schematic diagram of the XOR gate with 10 transistors

Reference

Sicard, E. (2017). Implementation of the 14-nm FinFET in Microwind. Application note on-line