Using the Global Delay Evaluation

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Global Delay Computing

At integrated circuit level, there exist a possibility to evaluate the delay of each interconnect, in a global way, thanks to analytical approximations. We implemented in Microwind version 3.1 very simple approximations of the delay within interconnects, using the following formulations [Sicard 2005]:

```
delay=0.43*Rline*Cline+0.92*(Rline*Cgate+Rd_mos*(Cline+Cgate))
```

with

delay = RC delay of the propagation, in s
Rline= resistance of the line (in ohm)
Cline = capacitance of the interconnect (in Farad)
Cgate = capacitance of the loading gates (in Farad)
Rd_mos = equivalent on resistance of the MOS device driving the interconnect

Click "Analysis" → "Global Delay Evaluation" within microwind to access to this command.

Example

The example of the complete delay calculation of each interconnect is displayed in figure xxx. The classification of each nodes by decreasing delay appears in the navigator window. The worst delay appears at node Y1, with a delay estimated to 412 ps.

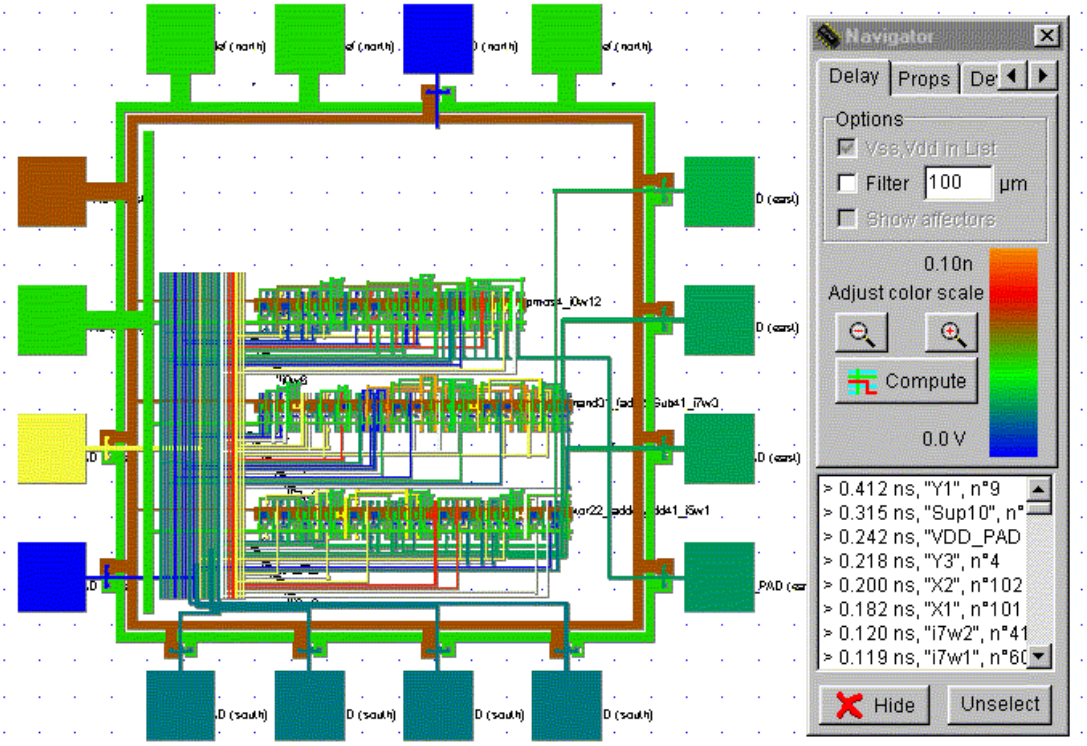

Figure 2 : RC delay estimation at chip level (AddBDC.MSK)

References

[Sicard 2005] E. Sicard, S. Ben Dhia Basics of CMOS cell design - Book published by Tata McGraw Hill, 450 pages, ISBN 0-07-0599335, June 2005

[Caignet 2001] F. Caignet, S. Delmas-Ben Dhia, P. Saintot, E. Sicard "The challenge of Signal Integrity in Deep Submicron CMOS technology", IEEE proceedings, April 2001, special topic "The future of Interconnects" Vol 89, N°4